MEMRISTIVE DEVICES

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1. INTRODUCTION

The emergence of the Internet of Things (IoT) and the insatiable demand for smart devices in every aspect of life is driving a complete overhaul of traditional wisdom in the microcontroller and embedded memory markets. The driving force behind the semiconductor industry is twofold: *(i)* Develop new material systems which exhibit novel or superior properties which can be exploited in various applications and devices. *(ii)* Decrease the size of constituent devices in order to make them more powerful and accessible to society.

The industry is currently facing barriers which will stall the scaling of memory and storage. In order to overcome these barriers, new materials and methods must be considered.

The NAND structure was introduced in 1987 by Dr. Fujio Masuoka from Toshiba. This structure uses a string of Electronically Erasable Programmable Read Only Memory (EEPROM) transistors connected in a series. NAND Flash technology has been serving the storage memory applications market for several decades – thus creating a dependency that has steadily increased due to its scaling technology.

Flash memory is a form of non-volatile EEPROM. Flash memory arrays consist of a grid of columns and rows, with two transistors at each intersection. A thin oxide layer separates the two transistors, known as the floating gate and control (external) gate (Figure 1). Flash memory cells work via the application of an electric field to the control gate. The field causes electrons to become trapped at the oxide-floating gate interface. A value of 0 or 1 is assigned to the memory cell based off of the shift in threshold voltage caused by the presence of electrons[1]. However, in recent years, further scaling of this technology has shown profound limitations.

Currently, it is widely accepted that scaling below 25 nm has significantly degraded performance and reliability, thus, resulting in significant overhead complexity and computational power-demand from the system controller. System manufacturers as well as NAND Flash manufactures have begun the quest for a new technological solution. For several years now, companies[2] have focused on developing a next generation memory technology that will lead to significant improvements in reliability, performance, low power operation and scalability compared to existing non-volatile memories.

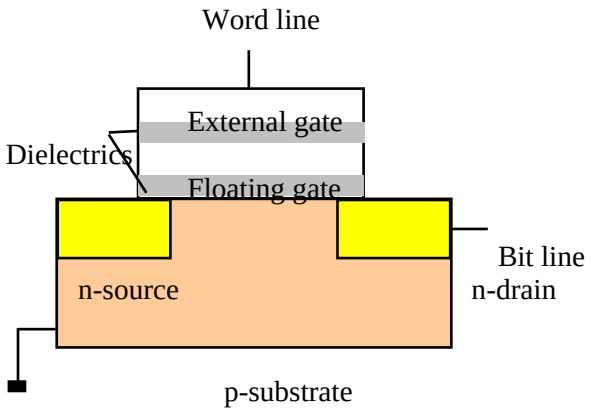

Figure 1. *Flash memory cell (after [1]).*

Several non-volatile memory device structures such as Ferroelectric RAM (FeRAM), Magneto-resistive RAM (MRAM), Organic RAM (ORAM) and Phase Change RAM (PRAM) have been proposed [3]. Resistive Random Access Memory, (RRAM or ReRAM), shows superior switching speeds, requires less power, exhibits high endurance, and is compatible with current CMOS manufacturing processes.

[1] However, current models of flash store a limited number of electrons within the thin oxide layer. Because the system is sensitive to fluctuations in charge density, the loss of a single electron from thermal contributions can lead to loss of retention. Further scaling of Flash technology will only exacerbate losses.

[2] RRAM-based disruptive technologies have been sited and chosen by major R&D corporations as the best potential replacement for NAND Flash. At IEDM 2010, Sungjoo Hong from Hynix stated that *"RRAM can be one of the suitable candidates for a storage application due to its possibility of multi-stackable crosspoints."* During the 2011 Flash Summit, SanDisk CTO Yoram Cedar presented this message: *"3D RRAM technology development shows the best promise for a scalable post-NAND technology".* Again, at the 2013 ISSCC, Tz-Yi Liu from SanDisk presented *"32 Gbit RRAM Memory Device in 24 nm Technology," where he stated that "RRAM has been considered one of the potential technologies for the next generation non-volatile* memory, given its fast access speed, high reliability, and multi-level capability." [2].

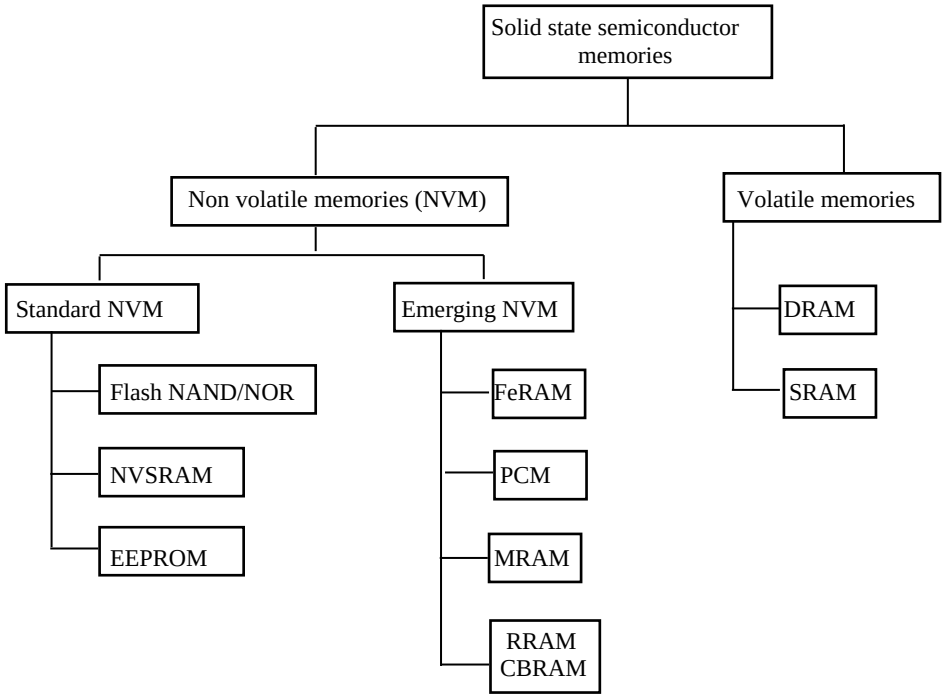

Figure 2. The solid state semiconductor family of memories. *CBRAM = Conductive Bridge RAM; DRAM = Dynamic RAM; FeRAM = Ferro Electric RAM; MRAM = Magnetic RAM; PCM = Phase Change Memory; RRAM = Resistive RAM [It can be also called Resistance Chance Memory (RCM)]; SRAM = Static RAM.*

Table 1. Comparison of memory and storage technologies [4**]**. Note that circuit-level overheads for the listed performance metrics are in general different among different device technologies and could often dominate individual device performance.*****

	Memristor	**PCM**	**STTRAM**	**SRAM**	**DRAM**	**Flash (NAND)**	**HDD**
	Prototypes				Commercialized technologies		
Reciprocal density (F2)	<4	4–16	20–60	140	6–12	1–4†	2/3
Energy per bit (pJ)	0.1–3	2–25	0.1–2.5	0.0005	0.005	0.00002	1–10 × 109
Read time (ns)	< 10	10–50	10–35	0.1–0.3	10	100,000	5–8 × 106
Write time (ns)	~10	50–500	10–90	0.1–0.3	10	100,000	5–8 × 106
Retention	years	years	years	As long as voltage applied	<< second	years	years
Endurance (cycles)	10^{12}	10^{9}	10^{15}	> 10^{16}	> 10^{16}	10^{4}	10^{4}

* The energy to operate NAND Flash is typically hundreds of picojoules (pJ) per bit primarily because accessing the memory cells requires charging word and bit lines to high voltages. †Smaller number represents an effective area for multi-level cells. PCM = phase-change memory; STTRAM = spin torque transfer random access memory; SRAM = static RAM; DRAM = dynamic RAM; HDD = hard disk drive.

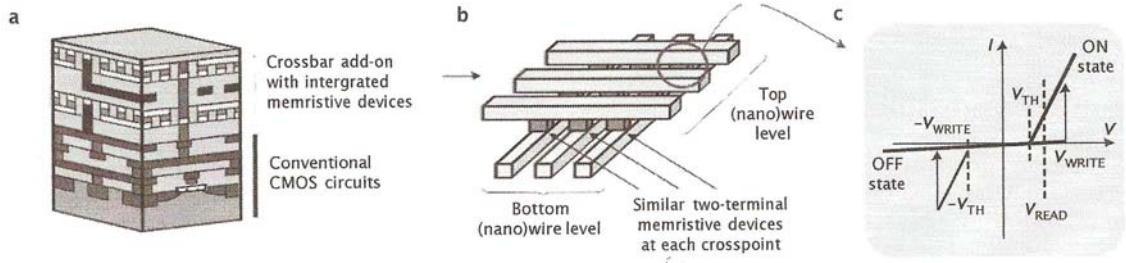

Figure 3. Hybrid CMOS/memristor circuits (**a, b**). *Owing simple functionality of memristors most practical approaches rely on combining memristors with sparse but more powerful conventional CMOS circuits **(a)** for example, by integrating memristive devices into crossbar structures on top of a CMOS subsystem. **(b)** Crossbar structures enable very high density in large-scale circuits, with devices defined by the overlap area of the two electrodes. **(c)** Schematic I-V curve for a nonlinear memristive device. V_{TH} denotes a threshold voltage below which current is negligible [5].*

2. SHORT HISTORY OF MEMRISTOR

Leon Chua - professor at UC Berkeley - discovered, in 1971 [6], a missing link in the pair wise mathematical equations that relate the four circuit quantities - charge, current, voltage, and magnetic flux - to one another. These can be related in six ways. Two are connected through the basic physical laws of electricity and magnetism, and three are related by the known circuit elements: resistors (connect voltage and current), inductors (connect flux and current), and capacitors (connect voltage and charge). But one equation is missing from this group: the relationship between charge moving through a circuit and the magnetic flux surrounded by that circuit - or more subtly, a mathematical double defined by Faraday's Law as the time integral of the voltage across the circuit [7]. Chua demonstrated mathematically that his hypothetical device would provide a relationship between flux and charge, similar to what a nonlinear resistor provides between voltage and current. In practice, that would mean the device's resistance would vary according to the amount of charge that passed through it. And it would remember that resistance value even after the current was turned off.

3. MEMRISTANCE

We now know that memristance is an intrinsic property of any electronic circuit. Its existence could have been deduced by Kirchhoff or by Maxwell, if either had considered nonlinear circuits in the 1800s. But the scales at which electronic devices have been built for most of the past two centuries have prevented experimental observation of the effect. It turns out that the influence of memristance obeys an inverse square law: memristance is a million times as important at the nanometre scale as it is at the micrometer scale, and it's essentially unobservable at the millimetre scale and larger [7]. As we build smaller and smaller devices, memristance is becoming more noticeable and in some cases dominant.

4. THE CROSSBAR

The crossbar (Figure 3) is an array of perpendicular wires. Anywhere two wires cross, they are connected by a switch. To connect a horizontal wire to a vertical wire at any point on the grid, you must close the switch between them. The HP idea was to open and close these switches by applying voltages to the ends of the wires. Note that a crossbar array is basically a storage system, with an open switch representing a zero and a closed switch representing a one. You read the data by probing the switch with a small voltage.

Like everything else at the nanoscale, the switches and wires of a crossbar are bound to be plagued by at least some non-functional components. These components will be only a few atoms wide, and the second law of thermodynamics ensures that we will not be able to completely specify the position of every atom [7]. However, the crossbar architecture builds in redundancy by allowing you to route around any parts of the circuit that don't work. Because of their simplicity, crossbar arrays have a much higher density of switches than a comparable integrated circuit based on transistors.

5. RESISTIVE MEMORY

The most promising emerging technology is Resistive Memory. In terms of nonvolatile memory (Figure 2), it is generally believed that transistor based Flash memory will approach the end of scaling within about a decade. As a result, novel, non-FET based devices and architectures will likely be needed to satisfy the growing demands for high performance memory and logic electronics applications. In terms of memory applications, it is generally believed that transistor based Flash memory will approach the end of scaling within about a decade. Hence one of the most important challenges in semiconductor industry is the need of a new memory technology which combines the best features of current memories such as high density of DRAM, fast speed of SRAM and non-volatile property of Flash with a CMOS compatible fabrication technology.

Resistive RAM, although behind the others in development, is very promising. This type of circuit element behaves as a memristor (a term derived from memory and resistor), a device that was predicted to exist in 1971 as the fourth circuit element (in addition to the resistor, capacitor, and inductor). Memristive devices are attractive for a number of reasons: they are nonvolatile, they have fast switching speeds, and they can be integrated into a crossbar memory structure that offers the potential to scale to very high densities (Figure 3b).

Nonvolatile memories with ultimate density near 1 terabit/cm^2 are predicted because the individual memristor bits are envisioned to be densely packed and addressed by nanocrossbar arrays using a 10 nm x-y pitch. The memristor bits may be incorporated heterogeneously into a

conventional CMOS process, which is used to address, read, and write the memory array. Commercial devices based on this technology are currently in development and should be on the market within one or two years. These devices, although early in their development cycle, may provide a new high-density nonvolatile memory technology for future systems developers. The individual memristors have been shown to be radiation hard to both total ionizing dose and displacement damage; however, reliability and the integration with underlying CMOS must be evaluated further before these devices can be introduced into critical applications.

The search for new computing technologies is driven by the continuing demand for improved computing performance, but to be of use a new technology must be scalable and capable.

Memristor or memristive nanodevices seem to fulfil these requirements [they show excellent resistance switching properties such as fast switching time (<50 ns), high on/off ratio (>10^6), good data retention (>6 years) and programming endurance (>10^5)] they can be scaled down to less than 10 nm and offer fast, non-volatile, low-energy electrical switching. Memristors[3] are two-terminal 'memory resistors', regardless of the device material and physical operating mechanisms, that retain internal resistance state according to the history of applied voltage and current. They are simple passive circuit elements, but their function cannot be replicated by any combination of fundamental resistors, capacitors and inductors [3, 8]. Moreover, their microscopically modified internal state is easily measured as an external two-terminal resistance. Memristors were originally defined as components that linked charge and magnetic flux [3], but they can be more usefully described as devices with a pinched-hysteresis loop whose size is frequency dependent[3]. The natural computing application for such devices is resistive random access memory (ReRAM or RRAM), but their dynamical nonlinear switching also suggests that they could be used to develop alternative computer logic architectures.

Memristive devices can be classified based on switching mechanism, switching phenomena or switching materials. Here we loosely group all ionic switching devices into two categories - anion devices and cation devices - to simplify the discussion of their mechanisms.

Research activity in resistance switching has been primarily driven by the search for an ideal memory device. Indeed, hybrid CMOS/ memristor circuits, and in particular those with the passive crossbar architecture, could potentially combine all the desired properties of 'universal memory' - high speed, low energy and high endurance of static random access memories, and high density, low cost and non-volatility of lash memories (Table 1).

RRAM is a two terminal device that the switching medium is sandwiched between top and bottom electrodes (Figure 4) and the resistance of the switching medium can be modulated by applying electrical signal (current or voltage) to the electrodes.

The resistance switching effect has been observed in a broad range of materials such as perovskite oxide (e.g. $SrZrO_3$, $LiNbO_3$, $SrTiO_3$) [9-11], binary metal oxide (e.g. NiO, CuO_2, TiO_2, HfO_2) [12-18], solid electrolytes (e.g. AgGeS, CuSiO) [19, 20] and even in some organic materials [21-23].

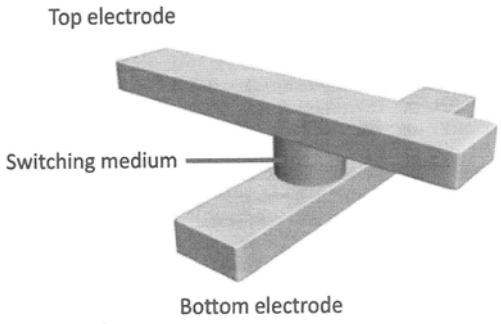

Figure 4. Two terminal RRAM structure. The resistance of a switching medium determines the state of the device [2].

The crossbar structure (Figure 5) consists of an array of parallel bottom nanowire electrodes, an array of parallel top nanowire electrodes with 90° degree with respect to the bottom electrodes and the switching medium between the electrodes. Each cross-point formed at the intersections of the top and bottom electrodes corresponds to an individual RRAM cell [2].

As digital memory devices, the devices are ideally suited in the crossbar architecture which offers ultra-high density and intrinsic defect tolerance capability. As an example, a high-density (2 Gbits/cm^2) 1 kb crossbar memory was demonstrated with excellent uniformity, high yield (>92%) and on/off ratio (>10^3), proving its

[3] Any two-terminal electronic device devoid of internal power source and which is capable of switching between two resistances upon application of an appropriate voltage or current signal, and whose resistance state at any instant of time can be sensed by applying a relatively much smaller sensing signal, is a *memristor* [6].

promising aspects for memory and reconfigurable logic applications. Properly designed devices can exhibit controlled analog switching behaviour and function as flux controlled memristor devices [2].

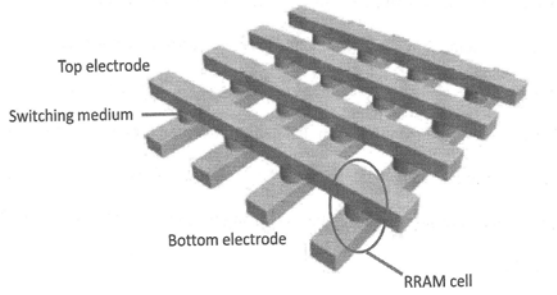

Figure 5. The schematic of a crossbar array (after [2]).

In essence, memristors operate as resistors the resistance of which can be changed and maintained in a non-volatile manner. This feature (and their compact size) is basically what makes them highly attractive not only for memories and computing systems in general, but also for building too neuromorphic systems. However, memristance is not necessarily restricted to two-terminal devices. It is well known that it is possible to use three (or four) terminal FETs (Field Effect Transistor) as resistors, current sources, or (volatile) memory elements. If the same nano scale principles that give rise to memristance in two-terminal devices could be extrapolated to three or four terminal FETs, then the adaptive memristive circuits presented so far could be extrapolated to more generic FET-based circuits as well. FETs have more terminals and consequently will result in less dense structures than their two-terminal counterparts. However, FETs can present very wide tuning ranges. For example, imagine a (nano)FET transistor in which the threshold voltage could be tuned through some memristive-like mechanism [24].

6. REQUIREMENTS TO FUTURE NON-VOLATILE DEVICES [25]

- *Energy efficiency*: Reset: < 100 μA; voltage$_{\text{-set, reset}}$ < 3 V
- *On/off ratio* >10
- *CMOS compatibility*: Read: ~1 μA, ~1V; J>10^6A/cm^2
- *Scalability*: <10 nm
- *Reliability*: Retention: 85°C 10 years; Endurance: >10^5@1 μs pulse

7. SOME RECENT APPLICATIONS

Memristive computing is a new area of research, and many of its fundamental questions still remain open. For example, it is yet unclear which applications would benefit the most from the inherent nonlinear dynamics of memristors. In any case, these dynamics should be exploited to allow memristors to perform computation in a natural way instead of attempting to emulate existing technologies such as CMOS logic. Examples of such methods of computation, presented in [26], are memristive stateful logic operations, memristive multiplication based on the translinear principle, and the exploitation of nonlinear dynamics to construct chaotic memristive circuits.

The main conclusion of [26] is that memristive computing will be advantageous in large-scale, highly parallel mixed-mode processing architectures. This can be justified by the following two arguments. First, since processing can be performed directly within memristive memory architectures, the required circuitry, processing time, and possibly also power consumption can be reduced compared to a conventional CMOS implementation. Second, intrachip communication can be naturally implemented by a memristive crossbar structure [26].

CMOS/memristor hybrid architectures combine conventional CMOS processing elements with thin-film memristor-based crossbar circuits for high-density reconfigurable systems. These architectures have received an explosive growth in research over the past few years due to the first practical demonstration of a thin-film memristor in 2008. The reliability and lifetimes of both the CMOS and memristor partitions of these architectures are severely affected by temperature variations across the chip. Therefore, it is expected that dynamic thermal management (DTM) mechanisms will be needed to improve their reliability and lifetime [27].

In order for CMOS/memristor architectures to become commercializable, several of their reliability concerns must be addressed. Due to their close proximity, memristor partitions of the architectures will be affected by thermal gradients in CMOS partitions. Due to their small feature sizes, temperature variations will have a significant effect on memristor crossbar circuits' performance and reliability. Therefore, these architectures will require dynamic thermal management (DTM) schemes to maximize device lifetimes and mitigate reliability concerns. DTM in traditional CMOS architectures has become a well established research domain. Currently, however, no work exists on thermal

management in next-generation CMOS/memristor hybrid architectures. Thesis [28] explores one aspect of thermal management–thermal profiling - in a CMOS/memristor hybrid memory architecture.

Memory circuit elements (namely memristive, memcapacitive and meminductive systems), are gaining considerable attention due to their ubiquity and use in diverse areas of science and technology. Their modelling within the most widely used environment, SPICE, is thus critical to make substantial progress in the design and analysis of complex circuits. Paper [29] presents a collection of models of different memory circuit elements and provides a methodology for their accurate and reliable modelling in the SPICE environment. The authors provide codes of these models written in the most popular SPICE versions (PSpice, LTspice, HSPICE) for the benefit of the reader. This will be of great value to the growing community of scientists interested in the wide range of applications of memory circuit elements.

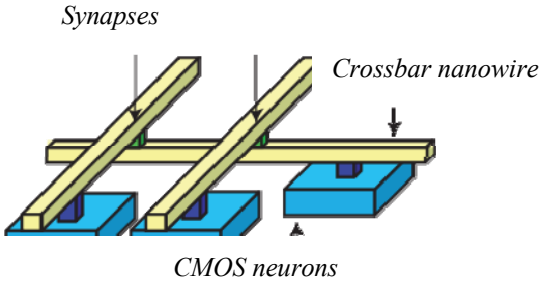

Figure 6. Bio-inspired and mixed-signal information processing: hybrid CMOS/memristor circuits may also enable efficient analogue dot-product computation, which is a key operation in artificial neural networks [5].

The idea of using resistance switching devices in artificial neural networks (Figure 6) and for mixed signal computing, in general, has a long history and can be traced back to at least the 1960s.

Synchronous memristive Spike-Timing-Dependent-Plasticity (STDP) learning architectures were proposed by Snider [30, 31], assuming voltage/flux driven memristors, and recently demonstrated by the group at Michigan University [32]. In that proposal each neural spike is mapped into a sequence of precisely spaced fixed amplitude digital pulses which must maintain global synchronization to separate the integration phase of neural activity from the synaptic weight update phase. This global synchronization requirement imposes severe difficulties when the system scales up to very large sizes.

8. CONCLUSION

Resistive RAM, although behind the others in development, is very promising. The development of memristive devices has recently witnessed remarkable progress. Nevertheless, it remains to be seen if memristive devices can combine all these characteristics in a single commercially competitive device design. Further research into device mechanisms - particularly the microscopic processes of the initial and subsequent switchings - is crucial to achieve reliable and predictable nanodevices at the wafer scale [5, 27].

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