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Failure Analysis and Reliability Aspects of Electronic Components

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Abstract

Failure analysis (FA) is the process of determining the cause of failure, collecting, and analysing data, and developing conclusions to eliminate the failure mechanism (FM) causing specific device or system failures. Why it is so important to use FA, i.e. to know the cause of product failure, this is what we intend to describe in this article. Reliability analysis is not at all the only 'customer' of FA. Other fields, such as business management and military strategy are using this term. In order to offer to the reader a more complete picture, we identified the possible applications of FA in various fields (industry, research, etc.), which are detailed in the article.

Keywords: Failure analysis, reliability, failure mechanisms, physics of failure

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Introduction

Reliability engineering is becoming increasingly important for the competitive success of industry.

Effective reliability estimation and improvement requires a fairly sophisticated set of skills.

The scaling down of devices in advanced VLSI circuits has created major reliability problems. Some of the mechanisms that are affecting the reliability of electronic devices are matchup, electrostatic discharge (ESD), hot carrier effects, thin dielectric breakdown, and electromigration. Screening and accelerated tests are carried to detect early life failures and estimate the mean time to failure of the product. Optimization of these tests is an important factor in maximizing the yield while maintaining the effectiveness of the tests.

The reliability parameter determines the time period during which a product will preserve its properties. According to generally available data, this period reaches 30 years in the space and medical industries, while in the military and civil industries it varies from 15 to 25 years.

Unfortunately, the Russian industry is unable to ensure comparably high reliability figures at present.

This situation is testified eloquently by more frequent accidents with the Russian spacecraft along with an increasing volume of claims raised by the consumers of high-tech products (HTP).

Research into the causes of failures showed that the most unreliable device elements are electronic components (EC).

For example [1], the utilized Russian-made and accessible foreign made EC (of commercial and/or industrial grade) are not able to ensure the required set of spacecraft specifications, nor terms of active orbital operations of spacecraft under the conditions of exposure to the space environmental factors. In particular, the satellites ensuring operation of the Russian GLONASS system remain functional for not more than 3 years, while the GPS components are able to operate actively up to 30 years [17].

Organisation of screening tests

One of the options in solving the problem of improving the reliability of a product electronic system is to organize a set of additional customer EC tests [17].

The set envisages the incoming inspection, screening tests, diagnostic non-destructive tests and random destructive tests. This will result in the rejection of the most unreliable components.

With a view of increasing the overall reliability of an electronic system, the multiple redundancy principle for the most critical components is applied when necessary and a partial load mode of EC operation is assigned.

In general, the incoming inspection is conducted in the scope of acceptance tests, including the appearance test and check of the electrical parameters reflecting the product quality.

The screening tests include burn-in testing, heat cycling and hot soaking. The diagnostic of non-destructive tests are conducted with informative parameters using the schedules and conditions promoting defect manifestation as well as based on the post-test parameter drift evaluation results.

The random destructive physical analysis is applied with a view to evaluating the preservation of EC design and process parameters.

Despite the measures implemented, the problem of reliability of electric components used in the fabrication of HTP electronic systems is still relevant due to a number of negative trends developing in the EC market.

The first trend relates to an increasing use of commercial components in military equipment (ME) due to a pressing necessity to cut the costs of product development and testing and to reduce production startup time.

The utilization efficiency of the industrial-grade EC in military products is compared to military and space-grade EC (Figure 1 [2]).

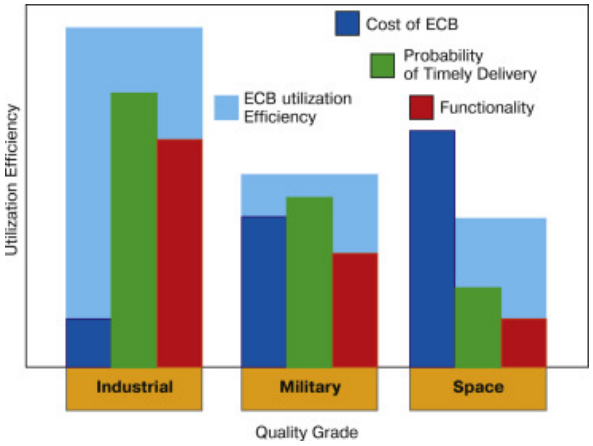


Figure 1. Utilization efficiency of industrial, military and space-grade EC in military products

As can be seen from Figure 1, the price of industrial-grade EC is substantially lower than that of military and space-grade EC while other parameters are significantly higher.

The second trend relates to an increasing presence in EC market of new companies from China, countries of the Southeastern Asia and other regions that produce components of questionable quality.

Thus, the US Defense Department was so concerned about more frequent failures in the operation of critical ME systems, that it prohibited the use of China-made EC [3].

The third trend consists in the increasing share of counterfeit products in the EC market. Today, this share is as high as 10%.

Considering the counterfeit EC available in the market and the low quality of foreign and domestic products supplied by intermediaries and unscrupulous companies, the ME manufacturers have to implement organizational and engineering measures to prevent EC of improper quality from getting into electronic equipment.

Articles [2], [4]-[10] provide descriptions of quality and reliability control procedures for the electric radio products (ERP) intended for the manufacture of space equipment.

Figure 2 shows a typical failure rate vs. time dependence for various EC.

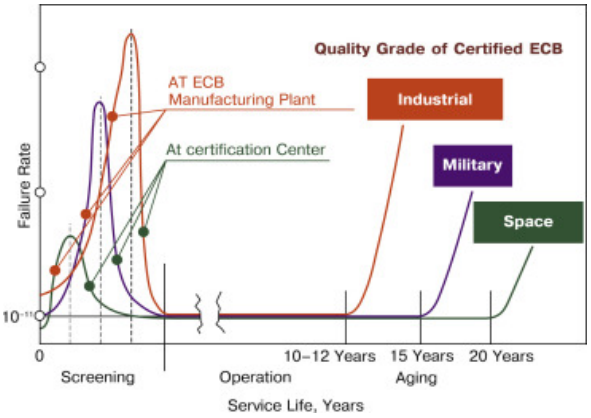


Figure 2. EC failure rate λ *vs* service life

At the first stage (screening), the failure rate increases first but then drops to a stable value upon reaching the maximum.

During the period of stable operation, the failure rate varies insignificantly.

At the third stage, the failure rate increases again due to the physical aging of the products. The points indicate two rejection procedures.

The first procedure is implemented at the EC manufacturing plant by QC departments. As can be seen from Figure 2, the time allocated for screening tests at the manufacturing plant is absolutely insufficient, and so the consumer receives components with high failure rates.

The second procedure is applied during the incoming inspection at the consuming plant or a certification centre. The screening performed during the incoming inspection includes EC burn-in testing. In this case, the burn-in conditions are determined by the composition and level of external effects. Each type of exposure provokes the development of certain failure mechanisms. To reduce time expenditures, EC burn-in testing is performed at elevated temperatures and voltage. Electronic components whose parameters during the burn-in testing were changed above the established standards are subject to rejection. Thus, EC with improper reliability is prevented from being installed into critical equipment.

It should be noted that burn-in conditions are selected so that to exclude new defects in ERP. In so doing, the screening procedure efficiency is increased if microelectronic products are additionally subjected to destructive physical analysis (DPA) [11].

The DPA includes:
- measurement of electrical and physical parameters,
- check for moisture vapor content inside the package,
- chip visual inspection,
- check for installation quality with the use of a scanning electron microscope,
- check for internal joint efficiency,
- shear test and other physical and chemical techniques.

Should any manufacturing defects be identified, either the production lot is to be rejected or the basic failure rate established for the EC under test is to be increased, depending on DPA criteria?

The certification tests conducted so carefully provide for the creation of databases on failure modes, failure statistics, circuit solutions with defects detected, and EC manufacturers with quality and reliability characterization.

Table 1 presents the most common failures and their causes.

Table 1. The most common failures and their causes

Failure	***Probable cause***
Package breakdown	Electrical and/or thermal overload
Electrical breakdown	Electrical overload, excessive moisture, contaminants
Mechanical damage	Deformation due to differing thermal expansion coefficients
Chip separation	Chip-to-substrate bonding defects
Breakdown of metallization layers	Electrostatic discharges, corrosion, electric and/or thermal overload
Electromigration	Flowing current
Damage to oxide layers	Electrostatic discharge, pores
Deformation	Mechanical stress during heat cycling
Chip defects	Defects in bulk semiconductors

During the destructive physical analysis, the following typical non-compliances with the design and process parameters are detected:
- excessive content of water vapours;
- flux residues and other contaminants on the chip surface;
- bound and loose foreign particles;
- corrosion;
- etched basic oxide areas;
- bridging between switching buses;
- poor chip-to-substrate attachment.

Due to an abruptly decreased or rather almost completely discontinued production of radiation-resistant EC, satellite system designers had to use commercial-grade EC.

It is obvious that these components are not so reliable and possess a lower radiation resistance. In other words, the presence of defects is much more likely for commercial-grade EC than for those manufactured using a special "radiation-resistant" technology.

This problem can only be solved through the rejection of faulty components (or selection of high-quality products out of the production lot) [12].

It is well-known that over 60 % of failures in CMOS integrated circuits are caused by oxide film defects. Experimentally, it was determined that some structural defects can form defect clusters — the macro-defects.

Charge accumulation in macro-defects during operation causes IC degradation and eventually results in IC failure.

It should be noted that macro-defects cannot be detected based on electrical measurements either after fabrication or after burn-in testing as they are electrically neutral.

The experiments proved that oxide film defects are charged efficiently upon exposure to ionizing radiation. Additional charging of macro-defects, if any in the film, also takes place during subsequent heat treatment at a preset temperature.

Thus, it was experimentally demonstrated that after irradiation and heat treatment, the EC parameters are restored, if there are no macro-defects in the oxide film and will not be restored in the contrary case — if macro-defects are present.

Selected EC with restored parameters can be used in space systems.

The above tests including the "irradiation heat treatment" step found their way into national standards of a number of countries.

It should be borne in mind that application of the radiation heat treatment is unable to identify all potentially unreliable EC and unpredictable in-service failures are still possible.

The problem is solved by introducing various types of redundancies:
- hardware,
- mode,
- information.

Information coding (e.g., the Hamming code) can be used as an example of information redundancy.

Cumulatively, the integrated application of various reliability improvement techniques even for commercial-grade products makes it possible to reduce the random failure rate to the level of space-grade requirements of $1\ 10^{-8}$-$1\ 10^{-9}\ h^{-1}$ in terms of EC.

Optimization of Electronic Component Structure

In this part, we will consider the reliability problems typical of EC fabrication subject to nanoscale standards.

It was noted at one of the world forums — the Annual International Electron Devices Meeting (December 6-9, 2010, San Francisco) — that the most critical aspect of innovative microelectronics is chip reliability as the new advanced technologies are not

able to guarantee the fabrication of highly reliable components [14]. This requires respective techniques for designing reliable electronic systems fabricated using EC with low reliability.

The following fundamental problems that determine the reliability of future chips regulated by nanoscale layout standards can be distinguished:

- Influence on primary treatment reliability and bias temperature instability;
- Influence on reliability of copper metallization and dielectrics with low k of the following factors: electric migration, formation of micropores due to mechanical stress and time-dependent dielectric breakdown (TDDB);
- Influence of down-scaling new architectures on the degree of device protection against electrostatic discharge.

Besides, the reliability is substantially impaired by the spread of chip component parameters, this spread being caused by thermodynamic variations of physical and chemical processes typical of the chip fabrication technology [15].

The primary process factors causing parameter variations are as follows:

- Non-uniform distribution of doping agents and structural defects in nanoscale semiconductor volumes and variation of dielectric layer thickness;
- Grain structure of metal and polycrystalline films;
- Distortions occurring during lithography.

There are several ways of reducing the influence of parameter variations on reliability.

One consists in the improvement of the fabrication technique and substantiation of the functional material selection.

The second way is the optimization of circuit solutions. For instance, parameter spread caused by non-uniform distribution of doping agents in the CMOS transistor structure can be reduced by increasing the agent concentration in the source and drain areas and its reduction in the gate area. In this case, the drain-source leakage currents through the substrate will increase.

To reduce this effect, the modification to a MOS transistor structure is needed consisting in the synthesis of an isolating dielectric layer.

It should be noted that as-cut silicon wafers with uniform distributions of phosphorus doping agent can be obtained by nuclear reaction doping [16].

The spread of such parameters, as gate-drain leakage current, threshold voltage and maximum open transistor current can be decreased by increasing the gate dielectric thickness with the proportional increase of its dielectric permeability.

In real structures, a two-layer dielectric is commonly used:

- The first layer is silicon dioxide with a thickness of about 1 nm,
- The second one is a mixture of aluminium oxide and hafnium or hafnium dioxide.

In order to reduce the influence of polysilicon with a pronounced coarse-grained structure on the spread of IC component parameters, titanium nitride, tungsten or tantalum silicide are used nowadays, instead of polysilicon that have an almost amorphous structure and are able to withstand process heat treatments without any changes.

For the reduction of conductor resistance, multilayer structures with a conductive copper layer are applied.

The network-on-chip VLSI architecture is an example of compensating process variations through the optimization of circuit solutions. In other words, the device chip represents a matrix consisting of tens or even hundreds of modules with numerous interconnections. This architecture provides a solution for such problems as energy saving, synchronization, continuous performance monitoring and maintenance of IC operation through the compensation of various destabilizing factors.

The estimation of geometrical parameters for a local computation module with structural components measuring 45 nm provides a geometrical region of (2 x 2) mm^2, within which up to 3×10^6 transistors and necessary signal connections can be accommodated.

It will be sufficient for implementing a basic processing unit with a local memory, a switch, and additional functional units. Not only the proposed NoC architecture provides the optimization of the overall system energy consumption, but for the enhancement of its reliability as well.

For this purpose, each module is provided with built-in control facilities, which are able to manage the operation mode and monitor the preservation of a correct functional module and chip in case of any variations in ambient temperature, cooling conditions or degradation of component parameters with time.

The reliability enhancement facilities embedded in the structure of modern VLSI circuits with nanoscale-level components are divided in three groups.

The first one includes logical facilities. These are code protection of memory units, interconnections as well as the implementation of distributed computing with a distinct, hierarchically distributed memory structure and optimal ways of accessing it. In case of no logical reliability assurance facilities are implemented, current consumption of the systems based on the processors operating at the maximum frequency will amount to up to 1000 A at a voltage of 1.0 V-1.2 V. Heat dissipation and chip current distribution problems will appear. Such VLSI circuits may simply be inoperable.

The second group includes integrated facilities controlling temperature, supply voltage, sync pulse frequency and bias voltage. In addition, control over leakage current, pulse noise level in power circuits and logic element delays is provided.

The third group includes facilities for controlling system reserves in the event when the error level goes beyond the preset limit owing to various destabilizing factors.

Control over reserves is implemented by the central control unit interconnected with built-in

control facilities of the former two groups.

If need be, the central unit decides on changing the NoC configuration and redistributing resources, which allows preserving system operability and ensuring its reliability under the conditions of exposure to destabilizing factors.

State of art

Today, the manufacturing of electronic components (EC) is the most dynamic process, because of the great demands imposed on the performance specifications of modem devices determine a quick rate of change for these products.

The electronic components and, especially, the semiconductor devices have always been thought as having the potential to achieve a high reliability and, consequently, the development of many quality and reliability techniques was made particularly for these devices.

Consequently, the reliability research on this field stands for the front line in the battle for the best products.

The evolution of the reliability field can be traced between the milestones of the semiconductor manufacturing history, as given by Birolini [15], Kuehn [48], Knight [46] and Bâzu [12].

The "new wave" in the reliability field, arrived after 1990, imposed some cultural changes, shown as the main features in Table 2.

Table 2. The evolution of the reliability field

Period	Main features	Domain
1945-1960	Normal tests on finite products	Final inspections
	Collection of reliability data	
	Failure analysis	
1960-1975	Accelerated life tests	Control
	Statistical process control (SPC)	
	Physics of failure	
	Reliability prediction	
1975-1990	Failure prevention	Assurance
	Process reliability	
	Screening strategies	
	Testing-in reliability	
After 1990	Total quality management (TQM)	Management
	Concurrent engineering (CE)	
	Building-in reliability	
	Acquisition reform	

These changes determine a new attitude toward the reliability field expressed by the approaches in the main domains concerning the reliability of semiconductor devices, domains listed in Table 3.

Table 3. Actual domains in the reliability of semiconductor devices

Cultural features	Quality and reliability assurance
	Total quality management
	Building-in reliability
	Concurrent engineering
	Acquisition reform
Reliability building	Design for reliability
	Process reliability
	Screening and burn-in
Reliability evaluation	Environmental reliability testing
	Accelerated life tests
	Physics of failure
	Prediction methods
Standardisation	Quality systems
	Dependability

Building-in reliability (BIR)

The implement of TQM requires changes in the organisational environment. An example is the role of the reliability group.

Traditionally, this group defined the testing requirements for a new product (correlated with operational conditions), performed the stress test and reported the final results.

Consequently, the reliability risk was assessed at the end of the development process, and it was difficult for the reliability group to be involved in the product development.

Only reactions to the development team were allowed, a team not containing the reliability group.

The lack of an integrated reliability effort leads to the cultivation of an organisational climate that recognises winners and losers in the new-product introduction process. This can lead to a tension between the new-product development team and the reliability engineering organisation that further limits its access to the new-product development process. Hence, the reliability group focused on reliability evaluation, which develops reaction, rather than anticipation skills, required by TQM.

Efforts were made on the way to surpass the weak points of the traditional approach to reliability improvement.

As the semiconductor devices become more reliable, the problem of ever rising costs and longer testing times begin to be recognised.

Building-in reliability (BIR) is a new concept, arrived in 27-29 March 1990, at the 28th edition of the International Reliability Physics Symposium held in New Orleans, Louisiana (USA).

There is a shift in focus within the semiconductor reliability community from the traditional reliability measurement models to building-in reliability. It was felt that improvement in reliability can only be realised if emphasis is placed on identifying and controlling the critical *input* variables (process and control parameters) that affect the output variables (such as failure rates and activation energies) [10].

The process of implementing the BIR begins with looking at output variables and then working backwards to identify the key input variables that impact the output variables.

Eventually, the identified input variables are monitored and a stable process in manufacturing is obtained.

Experimental results proved that BIR is an effective approach [38].

The core elements of a BIR approach are listed in Table 4.

Table 4. The core elements of a building-in reliability approach

Element	Details
Proact rather than react	Identify and eliminate or control the causes for reduced reliability rather than test for and react to the problem
Control the input parameters	Control the input parameters of the process rather than test the results of the process
Integrate the reliability	Integrate the reliability driven considerations into all phases of manufacturing
Asses the reliability	Asses the reliability of the product on the basis of a documented control of critical input parameter and of the reliability driven rules

For semiconductor devices, the BIR principles require an understanding of all elements related to:

The implement of a BIR approach involves too many cultural changes and too many segments of semiconductor and allied industries to evolve quickly enough without significant assistance.

Consequently, for the next years, testing-in reliability (TIR) approach remains an important tool and a complement even for a BIR technology. This means that, together with the implementation of a documented control of the input parameters, the reliability must be tested and monitored on the manufacturing flow[1].

Concurrent engineering (CE)

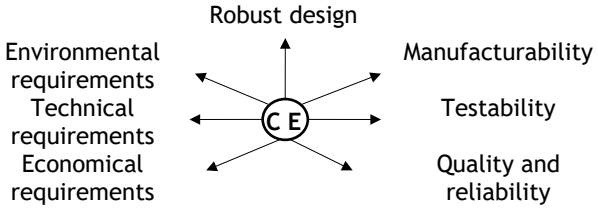
Concurrent engineering (CE) is a DoD (Department of Defence of USA) initiative for the Defence industry, successfully used, too, by commercial industries.

> It is a systematic approach to the integrated concurrent design of products and their related processes, including manufacture and support. This approach is intended to cause the developers, from the outset, to consider all elements of the product life cycle from conception through disposal, including quality, cost, schedule, and user requirements. (MIL-HDBK-59, Dec. 1988).

As Hoffman [2.40] points out, the CE must include business requirements, human variables, and technical variables.

All these elements are presented in Table 5 and must be taken into account starting with the design phase.

Table 5. Elements of a concurrent engineering (CE) analysis



The design team contains specialists from various fields, such as: designing, manufacturing, testing, control, quality, reliability, service, working in parallel. In fact, another name for CE is “parallel engineering”.

Each specialist works part time in a project, and he is involved at each phase of the developing process. A synergy of the whole team must be realised: the final result overreaches the sum of the individual possibilities.

Failure analysis (FA)

Failure analysis (FA) is a key method in any reliability analysis because failure fighting is the *raison d'être* for reliability as a discipline [1].

FA is the process of finding the causes of defects, collecting, and analysing data and conclusions are drawn on the elimination of failure mechanisms (FM) for devices or systems.

In the following, several possible applications are presented.

Investigation engineering

The *investigation engineering* term means the study of materials, products, structures, or components that fail or do not function properly, producing personal injury or damage.

As in any detective investigation, the research begins with the analysis of information about the “dead” or “damaged” product, i.e., defect reports or examples of previous defects of the same type of product.

For defective products, all storage conditions are checked first.

Then the “bodies”, i.e., the defective products themselves, are investigated.

The analogy with medicine is obvious. Specific methods are used, such as in the case of electronic components, first electrical and mechanical characterisation (of the capsule), then, if the failure mechanism (FM) has not been identified, then increasingly more complex methods are used (electron microscopy, X-ray, spectroscopy, laser methods, etc.).

Again, as in forensic medicine, “witnesses” (those who have worked the manufacture of the component or used it), to identify possible faults in the human errors that led to the failure.

[1]The BIR focus is on uncovering and understanding causes for reduced reliability and on finding ways to eliminate or control them. In doing so, the approach offers not only new measures for product reliability, but also a methodology for attaining ever-greater product reliability.

If the failure resulted in human casualties or material damage, production is stopped when the root causes of the damage are identified. The discipline that deals with the consequences of failures is called *reliability*.

Another discipline involved in investigations can be *intellectual property*, which, as you know, refers to patents. Often, defects stem from the desire to apply a patent against the authors.

The ultimate goal of investigative engineering is to find the root causes "root causes of defects".

The solution to the immediate problem must be followed by corrective actions, which prevent future defects of the same type: changes in conditions and control conditions etc. [3].

This is the correct procedure in any FA.

A classic example of the correct application of corrective actions is the FA performed for the Apollo programme after the terrible event of 27 January 1967, which happened at a routine simulation of the Apollo 1 mode, which resulted in the entire crew perishing in a fire on the Saturn 1-B carrier rocket [3].

Only two years, 5 months and 23 days later, on July 20, 1969, the Apollo 11's lunar module "Eagle" successfully landed.

A significant detail: during FA performed for Apollo 1, the second capsule was sacrificed to accommodate the better understand what had happened and determine the fundamental root causes.

Burn-in

The burn-in method (no. 1015.2 of MIL-STD 883D) belongs to the first test category.

Its goal is to detect latent flaws or defects that have a high probability of surfacing as infant mortality failures under field conditions.

Although the major defects may be found and eliminated in the quality and reliability assurance department of the manufacturer, some defects remain latent and may develop into *infant mortality failures* over a reasonably short period of operation time (typically comprised among some days and a few thousand hours).

It is not so simple to find the optimum load conditions and burn in duration[2] , so that nearly all potential infant mortality components are eliminated. There must be a substantial difference in the lifetime of the infant mortality population and the lifetime of the main (or long term) wear out population under the operating and environmental conditions applied in burn-in [2.43].

The situation may differ depending on the state-of-the-art components, on the new technologies, on the custom-designed circuits.

The trend is towards monitored burn-in [2.60].

The temperature should be high, without to exceeding +150 °C, for the semiconductor crystal.

A *clear distinction* must be made between *test* and a *treatment*.

A test is a sequence of operations for determining the way a component is functioning, also a trial with questions previously formulated, from which no certain response is expected.

That is why the test time is short and the processing of the results is immediately made. It is an attributive trial, which gives us information about the type good/bad.

As treatment, the burn-in must eliminate the early failures, delivering to the client the rest of the bath-tub failure curve.

We distinguish three types of burn-in:

- *static* burn-in temperature stresses and electrical voltages are applied; all the component outputs are connected through resistors to *high* or *low*.
- *dynamic* burn-in temperature stresses and *dynamic* operation of components (or groups of components).
- *power* burn-in operation at maximum load and at different ambient temperature (0...+150°C), also the function test under the foreseen limits of the data sheet for +25 °C.

It is often difficult to decide when a static or a dynamic burn-in is more effective.

Should surface, oxide and metallisation problems be dominant, a static burn-in is better; a dynamic burn-in activates practically all failure mechanisms?

That is why the choice must be made based on practical results.

The *static* burn-in is utilised as control selection, by the manufacturers, and by the users.

Usually, according to MIL-STD 883D, a temperature of +125 °C, for 168 hours, is applied.

From all the six basic tests specified by the method 1015.2, the methods A and D are the most utilised (min. 168 h at the specified temperature).

The condition A foresees a static burn-in (only the supply voltages are present, so that the maximum junction number can be polarised). This type is applied particularly if utilised together with cooling, to bring forward the surface defects.

The condition D is frequently utilised for integrated circuits. The clock signal is active during the whole burn-in period and exposes all the junctions as much to the direct voltages, as to the inverse voltages. All outputs are loaded to the maximum allowed value.

The direction in which the bias is applied will influence the power dissipation and consequently the junction temperature of the device.

However, in complex devices there is very little distinction between stresses resulting from the two biasing methods since it becomes increasingly difficult to implement a clear-cut version of either option.

The *static* burn-in is particularly adequate for the selection of great quantities of products and is

[2] Any application of a load over any length of time will use up component lifetime; there can easily be situations where burn-in can use up an unacceptable portion of the main population lifetime.

simultaneously an economic proceeding.

The distribution is dominated by the surface-, oxide-, and metallisation-defect categories, resulted from some type of contamination or corrosion mechanism[3].

The continuously growing number of LSI and VLSI ICs (memories, microprocessors) has essentially contributed during the last time in disseminating the *dynamic* burn-in, while the load can be easily regulated, the tests can be programmed and continuously supervised, memorised, and the tests results can be automatically and statistically processed.

The selection temperature usually varies between +100 °C and +150 °C. Beyond a certain duration (comprised normally between 48 hours and 240 hours, depending on component and selection parameters), no more failure diminishing occurs.

The applied burn-in voltage depends also on duration. So, the same result can be obtained with the applied nominal voltage after 96 hours, or — with a superior applied voltage — after only 24 hours. But — as in the case of temperature — the limit values must not be exceeded.

Process reliability

A manufactured device is a collection of failure risks, depending on a large variety of factors such as quality of materials, contamination, quality of chemicals and of the packaging elements, etc. It may be noted that these factors are interdependent and, consequently, the failure risks may be induced by each technological step or by the synergy of these steps [2.8].

The different constitutive elements of an electronic component (die, package, and encapsulation) are coated with a metallic layer in the aim to fulfil the prescriptions in accordance with their requirements, and to guarantee a high operational reliability.

The most important phases of the component manufacturing are:

Die bonding to the package:

- Wire bonding from the conductive arias of the semiconductor die to the conductive surface of the package;
- Electrical soldering (or Zn soldering) of the package on the socket.

The chemical structure and the cleanliness of the gold layer of the package and of the die influence decisive all the manufacturing methods for semiconductor components.

Other important aspects are: the capacity of the semiconductor die to transfer the heat to the heat sink and the soldering resistance of the electrical connections.

To control a manufacturing process means to keep in time the quality of this process, so to assure the reliability of the process.

The operations that must be made are: evaluation, optimisation, qualification and monitoring.

An optimal process is first qualified and then, with the aid of the monitors, the process can be kept under control.

A specific tool is used for the evaluation, namely the statistical process control (SPC), containing such tools as: cause-effect diagrams (Ishiqawa), Pareto diagrams, ANalysis Of VAriance (ANOVA) etc.

To optimise the process, the Design of Experiments (DoE) must be used. After the process is statistically controlled, one can act for the continuous process improvement (CPI, or Kaizen, in Japanese), based on SPC.

Recent studies suggest the use of test chips as an instrument for monitoring the quality of each manufacturing step of VLSI chips and as a cost-effective procedure for eliminating potentially "bad" wafers.

The long-term reliability is estimated on the basis of the test chips manufactured on the same wafer as the fully functional chips.

In the 70's, Schroen et al. [2.78] suggested the use of new test structures which had been developed process monitoring. By stressing these reliability test structures, used earlier in the process and sensitive to specific failure mechanisms, more accurate information about the reliability of the devices would be obtained and in a shorter time than possible by the use of traditional methods. Because test structures are used, the extrapolation of the results to the device level must be cautious.

From 1982, the Technology Associates initiated annually the wafer level reliability (WLR) workshop where the concept WLR was developed.

Tools allowing to investigate the reliability risks at the wafer level and to monitor the process factors affecting the reliability were created.

In a more general sense, WLR problems are included in the process reliability concept. Hansen [2.41] determined with a Monte Carlo simulation model the effectiveness of estimating the wafer quality, in terms of wafer yield. Reliability predictions can be obtained from wafer test-chip measurements.

Reliability modelling

Modelling the time and demand dependence of the failure rate (for components) or MTBF (for systems) is one of the main purposes of reliability analysis for these reasons:

- The existence of such models makes it possible to extrapolate the results obtained by reliability testing beyond the test duration;
- The reliability level of the product can be estimated from the design phase in different

[3] Other defects include wire bond problems resulting from intermetallic formation and oxide breakdown anomalies. *Dynamic operation* results in higher power dissipation, current densities and chip temperature that the static burn-in configuration.

applications, a fundamental requirement for modern manufacturing instruments.

It is often difficult to decide when a static or a dynamic burn-in is more effective.

Should surface, oxide and metallisation problems be dominant, a static burn-in is better; a dynamic burn-in activates practically all failure mechanisms?

That is why the choice must be made based on practical results.

Reverse engineering

Originally, the reverse engineering was a tool for investigative engineering.

The concept was developed for electronic components, and then used for systems. It was called *reverse engineering* because it started from the finished product and worked backwards through the manufacturing flow to find out the possible causes of failure, all the way to design. Obviously, the main tool used was FA.

Over time, the success of this procedure made it attractive for another purpose, namely "industrial and military espionage".

By reverse engineering, you can "dismantle" any software product or hard product, so that the technological principles (design, processes, controls) can be identified and can be manufactured without buying the manufacturing license.

Over time, many small companies specialised in such activities.

During the communist period in Romania, when we were completely legally decoupled from technologically advanced regions, engineering was the main method of product development. Samples were bought, which were carefully analysed with FM methods, and the structure and technological process necessary to obtain the respective product were determined.

Today, the reverse engineering is used not only for espionage, but also for recovery of lost documentation, analysis of possible copies of patents, for the necessary payment, but also for teaching purposes.

Other uses

We summarise the various other uses of FA, some of a technical nature, others with economic, and finally, others of a managerial nature.

Control of critical input variables

For electronic systems, the main input variables are the parameters of the components used. FA is used for identify possible weaknesses, often after reliability tests on the components purchased for use in systems.

In the case of electronic components, the input variables are material parameters used. Again, reliability tests followed by FA can identify possible risks of reliability risks, especially for the manufacture of high reliability components.

Design for reliability (DfR)

It is the modern concept of the product design, which considers, from the design phase onwards, the entire development flow, the reliability requirements of the product. The basic idea is "it is better to operate before the event, than to re-operate" [1].

Everything is based on the knowledge of reliability risks for similar (or close) products, being design team to have a reliability specialist on the design team, who will be responsible for FA methods and be able to analyse the results.

A "robust" design is created, based on [5]:

i. Development of a function to anticipate possible deviations in the manufacturing flow;
ii. The design is relatively immune to these deviations. In principle, one goes from evaluation and repair to anticipation and design.

Process enclosure

By using Defect Physics (DF), both the design and the manufacturing process can be qualified, thus ensuring that the integrity of the reliability process is not compromised.

In high-volume production, a system of reliability monitors allows continuous improvement of the reliability level in a manufacturing node, including reliability testing, followed by FA (electrical characterisation, but also complementary methods).

The basic concept for reliability enhancement is to ensure reliability [1].

Saving money through early inspection

Controls during manufacturing should be carried out as early as possible. The reason is economic: the amount saved by eliminating defective devices is maximised at the entry check and reduced on as the inspection takes place later in the manufacturing flow.

A cost comparison is shown in Table 1 for electronic systems.

It can be seen that for it is preferable to check the components used at the input and not the parts used at the output already equipped.

In this respect, a rule of thumb says that these costs increase by an order of magnitude as you go down the technological stream. This is the so-called rule of 10: if we note with C the cost of the defect identified at the component level, at the defective part level it becomes 10C, and at the system level it increases to 100C.

A synergistic approach

Finally, FA allows a synergistic approach to defects, taking into account the induced by each technological process step, but also the synergies with previous steps. FA also allows taking into account the synergy of factors environmental factors [6].

The most important elements:

- The design (robust design, design for reliability and testability).
- The processing (process monitoring, materials characterisation, screening).
- The testing (final testing, periodic tests).

Conclusion

Possible applications of FA have been identified in the article, showing the need to use this tool at all stages of product development, as well as on the during its use.

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Author's Biography

Titu-Marius I. BĂJENESCU was born in Câmpina (Romania) on 2April 1933.

He received his engineering training from the Polytechnic Institute of Bucharest.

He served for the first five years in the Romanian Army Research Institute including tours on radio and telecommunications maintenance, and in the reliability, safety, and maintainability office of the Ministry of Defence (main base ground facilities).

R&D Experience: design and manufacture of experimental equipment for Romanian Army Research Institute and for air defence system.

He joined "Brown Boveri" (today: "Asea Brown Boveri") of Baden (Switzerland) in 1969, as a research and development engineer.

R&D *Experience*: design and manufacture of new industrial equipment for telecommunications.

In 1974, he joined "Hasler Limited" (today: "Ascom") of Berne as a Reliability Manager (recruitment by competitive examination).

Experience: set up QRA and R&M teams.

He developed policies, procedures and training.

He managed QRA and R&M programmes as QRA Manager monitoring and reporting on production quality and in-service reliability.

As a Switzerland official, he contributed to development of new ITU and IEC standards.

In 1981, he joined "Messtechnik und Optoelektronik" (Neuchâtel, Switzerland, and Haar, West Germany), a subsidiary of "Messerschmitt-Bölkow-Blohm" (MBB) of Munich,

as a Quality and Reliability Manager (recruitment by competitive examination).

Experience: Product Assurance Manager of "intelligent cables".

He managed the applied research on reliability (electronic components, system analysis methods, test methods, etc.).

Since 1985, he has worked as an independent consultant and international expert on engineering management, telecommunications, reliability, quality, and safety.

He is a university professor and has written many papers and communications on modern telecommunications, and on quality and reliability engineering and management.

He lectures as an invited professor, a visiting lecturer or a speaker at European universities and other venues on these subjects.

He is the author of many technical books, published in English, French, German, or Romanian languages.

His latest book, entitled (in German) *Zuverlässige Bauelemente für elektronische Systeme*, was published in 2020 by the prestigious publisher SPRINGER.

From 1991, he won many Awards and Distinctions, presented by the Romanian Academy, Romanian Society for Quality, Romanian Engineers Association, etc. for his contribution to the reliability science and technology.

Recently, he received the honorific titles of *Doctor Honoris Causa* from the *Romanian Military Academy* and from *Technical University of the Republic of Moldova*.

In 2013, he received, together with prof. Marius Bâzu (head of the Reliability Laboratory of the Romanian Research Institute for Micro and Nanotechnologies (IMT) the *Romanian Academy "Tudor Tănăsescu" prize* for the book *Failure Analysis*, published by John Wiley & Sons.

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