NN.5P GaP TEMPLATE BASED SEMICONDUCTOR-METAL NANOCOMPOSITE

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The development of powerful electronics depends on the progress in miniaturizing electronic components. However, the limitations of the fabrication techniques become an obstacle for the scaling down of conventional technologies. The interest in nanometer-scale materials and devices stimulated the development of alternative technologies in recent years. Metal nanowires are one of the most attractive materials because of their unique properties suitable for a variety of applications in nanoelectronics and optoelectronics. In nanoelectronic devices nanowires are used as interconnects, magnetic devices, chemical and biological sensors. The optoelectronic applications of metallic nanowires is based on the extended dielectric/metal interface, that can sustain the propagation of electromagnetic waves which are coupled to collective oscillations of the conduction electrons in the metal, so called surface plasmon polaritons, allowing the manipulation and transmission of light on the nanoscale. Metal nanowires can de fabricated with various techniques. One of the most cost effective of them is the electrochemical metal deposition. We report on the development of a pulsed electrochemical method for the deposition of Pt into a porous GaP template, and the utilization of the prepared metal/semiconductor composite as capacitance semiconductor device with improved capacitance-voltage characteristics.

The GaP porous semiconductor template shown in Figure 1 is produced by electrochemical etching of a 0.5 mm^2 region of an n-GaP substrate in a solution of H_2O:H_2SO_4 (50:20 volume units) at 40 ^oC under the applied bias of 25 V during 10 minutes. The diameter of the produced by this technology pores is around 500 nm, while the width of the porous skeleton walls is around 300 – 400 nm. The pores of the GaP template were electrochemically filled in with Pt by the application of voltage pulses. The parameters of pulses such as the amplitude, frequency and pulse width were optimized to assure a uniform deposition of the metal inside the pores. The image of the obtained Pt/GaP composite is shown in Figure 2.

The deposited Pt inside the pores in n-GaP forms a Schottky contact with the semiconductor skeleton. An advantage of the prepared Schottky diode is the huge interface surface which assures an increased range of variation of the capacitance of the diode under the applied reverse voltage. Another peculiar advantage of this geometry is the overlapping of the depletion regions inside the porous semiconductor skeleton at a certain applied reverse bias. This overlapping results in a rapid change of the device capacitance for a given change of the voltage. Semiconductor industry utilizes various structures and methods to implement variable capacitance semiconductor devices. Typically, the capacitance of these devices varies up to $1x10^{-4}$ pF per square micron per volt. The implementation of the prepared Pt/n-GaP nanocomposite as a Schottky varactor diode allowed us to reach a rate of capacitance change of $6x10^{-3}$ pF/V per square micron of the device surface and the variation of the capacitance from 12 nF to 2 nF with the applied bias change from 0.5 V to 4 V. The performances of the device can be further improved by optimizing the design and technology of metal deposition inside the semiconductor porous nanotemplate.

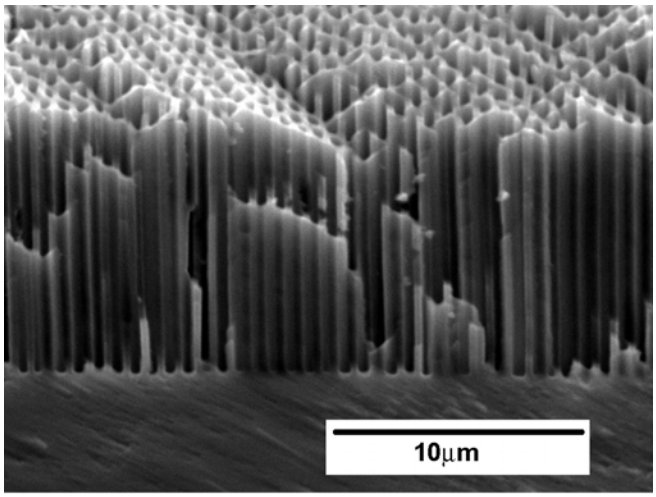

Fig. 1. SEM image of an initial GaP template.

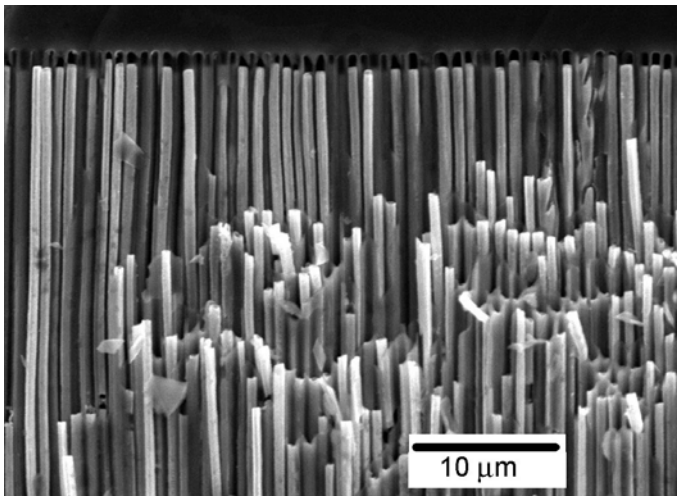

Fig. 2. Cross sectional SEM image of a Pt/GaP composite.