SSNN O7 CONTROL OF HVPE GROWN GaN NANOSTRUTURING BY ANODIZATION

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Gallium Nitride (GaN) is a wide-bandgap semiconductor compound (E_g = 3.4 eV at 300 K) with wide applications in electronics and solid-state lighting. Most of the devices were developed on GaN layers grown on foreign substrates by metal organic chemical vapor phase deposition (MOCVD) technology. The growth of bulk GaN substrate material by hydride vapor phase epitaxy (HVPE) technology was under intense exploration during the last decade. Fabrication of porous structures with controlled porosity was demonstrated in GaN for different applications, for instance for the fabrication of Bragg reflectors [1]. However, the prospects for the preparation of porous structures in HVPE grown GaN remains even less explored, since the quality of the produced material still requires substantial improvement. In this paper we report on elaboration of technological conditions for preparation of porous GaN structures with controlled morphology by anodization of HVPE grown substrates.

It was previously observed that the HVPE-grown GaN is usually inhomogeneous both on the surface and in the bulk due to peculiarities of the growth process, which is governed by the formation and subsequent overgrowth of the so-called V-type defects or pits on the film surface [2]. The produced topologies after electrochemical etching are due to the spatial modulation of the electrical conductivity throughout the surface and the volume of the HVPE-grown GaN wafer, resulting from non-uniform incorporation of the dopant during the growth process. We found that the nanostructuring of the HVPE-grown GaN wafer under anodization proceeds in different ways on the N-, or Ga-faces. Nanostructuring of the N-face requires anodization voltage in the range of 5-20 V, while application of voltages up to 100 V is required for the Ga-face. These differences are explained by different conductivity of the material near the two wafer surfaces.

In this paper, results of a systematic study of morphologies obtained with anodization in HNO_3, HCl, and NaCl solutions are presented. It is shown that complex pyramidal structures composed by regions with modulated porosity parallel to the pyramid surface, with pores oriented perpendicular to the wafer surface, or with arrays of nanowires are produced near the N-wafer surface, depending on the applied anodization voltage and the used electrolyte. Both current-line oriented pores and crystallographic pores are obtained by adjusting the anodization voltage. In contrast to this, porosification on the Ga-face proceeds from some imperfections on the surface, and develops in the depth porous matrices with pores oriented perpendicularly to the wafer surface. The thickness of the pore walls is controlled by the applied voltage. Porous matrices with the depth up to 50 μm have been demonstrated.

The quality of the porous material has been investigated by EDX analysis and high resolution scanning transmission electron microscopy (HRSTEM). The EDX analysis demonstrated the stoichiometric composition of the porous skeleton, while HRSTEM analysis of GaN nanowires and nanobelts revealed the crystalline wurtzite structure.

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