Time Delay Evaluation in Printed Circuit Boards based on Timed Hard Petri Nets

Sudacevschi Viorica, Ababii Victor
Informatics and Systems Engineering Department
Technical University of Moldova
Chisinau, Republic of Moldova
Viorica.sudacevschi@calc.utm.md,
Victor.ababii@calc.utm.md
Calugari Dmitri, Bordian Dimitrie
"Computer Science, Electronics and Communications"
Doctoral School
Technical University of Moldova
Chisinau, Republic of Moldova
Dmitri.calugari@scec.utm.md,
Dimitrie.bordian@scec.utm.md

***Annotation* – This paper presents a synthesis method for delay time evaluation in the printed circuit boards based on Timed Hard Petri Nets. For the specification and modeling of the delay time evaluation system, Timed Synchronous Petri Nets (TSPN) are used. The transition to the hardware description of the system is achieved by translating the TSPN into Timed Hard Petri Net (HTPN). The implementation of the delay time evaluation system is done by direct mapping of the HTPN into the reconfigurable hardware architecture (FPGA).**
***Key words* — printed circuit boards; Timed Hard Petri Nets; delay time; HDL; FPGA.**

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