FAILURE ANALYSIS IN DEVELOPMENT, MANUFACTURING, AND UTILIZATION OF A NEW ELECTRONIC PRODUCT

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1. INTRODUCTION

Failure Analysis (FA) is the process of determining the cause of failure, collecting and analysing data and developing conclusions to eliminate the failure mechanism (FM) causing the specific device or system failures. FA is the scientific method for identifying the cause that does not allow to a product to fulfil, during operation, the required function; in other words, making the device to fail. The goal of FA is to determine the root cause of a failure or parameter excursion so that corrective action can be taken. Understanding the cause of the part failure allows for effective corrective action and the prevention of future occurrences. When electronic parts fail, it's important to understand why they failed. Effective root cause analysis of part failures is required to assure proper corrective action can be implemented to prevent reoccurrence. Determination of root cause is also important for each high reliability system.

How did you learn FA? You took your background in physics, electrical engineering, biology, chemical engineering, or chemistry, and were thrown into the laboratory for your on-the-job-training. You read abundantly specialized international journals, attended tutorials, and found two or three good books, updated the field for leading edge techniques, retaining the tried and new methods, gaining a common understanding of the basic physics and electronics of the chips to be analysed. The major changes of the last decade is that the deep submicron technologies got deeper; from 0.25 μm to 90 and 65 nm technologies; and that brought not only small feature size and huge numbers of devices on a die, but new materials. Copper, low-k and high-k dielectrics, white LEDs based on phosphor conversion, and SOI or SoC are some of the examples of rapid challenge to failure analysts.

Imaging techniques had to respond to the challenge of observing materials whose minimum features were smaller than the shortest wavelength of visible light.

FA is now visibly a science requiring speciality teams.

How does an experienced FA engineer crack a tough analysis? What makes the difference between a new engineer's FA approach and the seasoned, effective analysis method of a veteran? Can our industry capture a formulation of correct FA methodology to accelerate the development of new engineers?

Electronics is so pervasive and necessary today that virtually every product either contains an electronic module or interfaces with one[1].

Today, for a FA, we have to analyse not only discrete passive components, but a great range of ultra-high density ICs too, with a huge design complexity that exceeds 500 millions gates and a great variety of technologies (bipolar silicon, CMOS, BiCMOS, GaN, SiC, complex heterojunction structures and microelectromechanical systems). That is why the today's analyst faces complex equipments sets (curve tracer, optical microscope, decapsulation tools, X-ray and acoustic microscopy, electron and/or optical and/or focused ion beam tools, thermal detection techniques, the scanning probe atomic force microscope, surface science tools, a great variety of electrical testing hardware etc.) that are necessary to realize a spatial and complex failure analysis. One sees that FA is a highly technical activity with increasingly complex, sophisticated and costly specialized equipments. It is very difficult to realize a balance between customer satisfaction, cost-effectiveness and future challenges. Very oft the analyst must make with a Today, in the domain of electronic components, it is almost impossible to conceive a serious investigation into the reliability of a product or process without FA. The idea that failure acceleration by various stress factors (the key to accelerated testing) could be modelled only for the population affected by the same failure mechanisms (FM) greatly promoted FA

[1] The merits and capabilities of solid-state semiconductor materials were discovered, developed and commercialized within the relatively short span of 60 years. Primarily drived by the requirements of the aerospace industry, the constantly increasing payloads of electronics demanded that miniaturization, reduced power consumption, and increased reliability of onboard navigation, weapons control, and communication equipment be pursued.

as the only way to segregate such a population damaged by specific FMs.

Moreover, the simple statistical approach in reliability, which was the dominant one for years, is no longer sufficient. The physics-of-failure (PoF) approach is the only one accepted at world level, being the solution for continuously improving the reliability of the materials, devices and processes. Even for the modelling of FMs, the well-known models based on distributions like Weibull or Lognormal have today been replaced by analytical models that are elaborated based on an accurate description of the physical or chemical phenomena responsible for degradation or failure of electronic components and materials.

In FA, a large range of methods are now used, from (classical) visual inspection to expensive and modern methods such as transmission electron microscopy, secondary ion mass spectroscopy and so on.

2. MANUFACTURING

Manufacturing is concerned with everything necessary to produce a product; this includes all of the realization processes, and those affected beyond, such as sales, service, recycling and so on. By definition, any product has to be producible; however, there are degrees of case or difficulty of manufacturability. These are caused by the difficulties of replicating the design, the effectiveness of the prototyping process to uncover problems, and the efficiencies of the manufacturing process. A producible design considers all of the factors that can affect how component parts are fabricated and assembled, how subsystems are fitted together, and overall product performance.

All products have a degree of functionality. How well products perform their intended functions depends – to a large extent – on how close the production version is to the original design and/or final design intent, based on the development experience with a prototype. The potential accuracy of the design is also important. Manufacturing is usually based on a sequential occurrence of events, specified so that previous steps will provide a robust foundation and path for succeeding stages.

Within the zero defects philosophy, different degrees of fault identification and tolerance must be established. This will allow design trade-offs to be made so that a minimum fault tolerance can be maintained without adversely affecting short- and long-term reliability, certain trade-offs have to be made.

Within airframe manufacturing cycle, every fabrication, inspection, and assembly station has supplier-customer interfaces, both of which have to sign off on the process accuracy and functional performance. There other systems helping this process, among them relational databases, which contain all product information, performance standards, process capabilities and material specifications. Updated continuously and instantly, these databases allow for continuous process improvement. Outside suppliers are also part of this manufacturing quality system. Industry quality standards are utilized so that common terminology and testing methods conform to worldwide requirements, resulting in completely integrated manufacturing.

3. FA TECHNIQUES

The basic flow for effective part FA starts before the component is removed from the board. Upon completion of the board troubleshooting and fault isolation process, the cognizant FA engineer should review the troubleshooting results while the part is still on the board witnessing any in-situ part measurements (for later verification in the FA lab) and noting any anomalies that exist on the board which may potentially have contributed to the part failure. Prior to removing a part from the board, it is also recommended to photograph the part as installed for future reference. Photos should be taken from various angles to capture the details of the installation, such as the solder attachment. In addition, contacting the vendor before removing high value parts is advised. Reviewing the failure data with the vendor can often identify external interfaces as the culprit rather than the suspected part. As some devices can cost many thousands of Euros to replace, it is highly recommended that all resources available be used prior to replacing them.

ICs are the central component to be analyzed. The manufacturing of silicon-based circuits is the central theme of this analysis. Other components in the typical electronic system (output, display, storage, input transfer, and power) are considered to be performing functions that are peripheral to the IC.

The failure analyst should also be consulted on the safest means for removing the part to preserve it to the greatest extent possible. Once the part is removed for FA, three basic processes should be followed:

• Electrical testing and part characterization. (test / characterize over temperature; curve tracer I-V check of inputs).

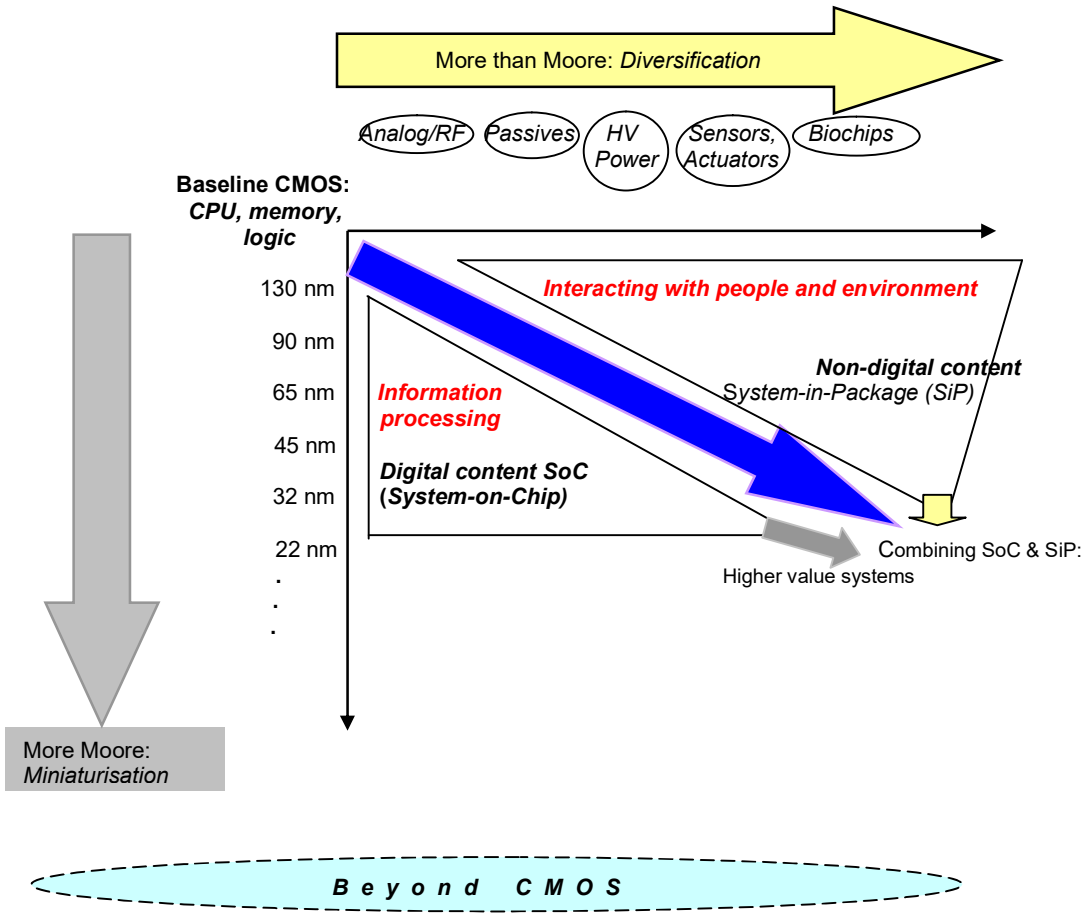

Figure 1. More Moore and more than Moore [Source: ITRS, ExecSum (2005)]

Non-invasive tests [external microscopic examination / photo fine and gross leak; vacuum bake (non-hermetic parts); X-ray; particle impact noise detector (PIND); X-ray fluorescence (XRF); scanning acoustic microscope (SAM); C mode-SAM (CSAM)].

• Invasive tests (lid removal / decapsulating; die examination; die probing; infrared microscopic examination; liquid crystal; cross-sectioning; scanning acoustic microscope (SEM); energy dispersive X-ray spectroscope (EDS); focused ion beam (FIB); Auger; secondary mass ion spectroscope (SIMS); Fourier transform infrared spectroscope (FTIR); transmission electron microscope (TEM); scanning transmission electron microscope (STEM).

4. STATE OF THE ART; FUTURE TRENDS

At component level, a broad definition of FA includes: collection of background data, visual examination, chemical analysis, mechanical properties, macroscopic examination, metallographic examination, micro-hardness, scanning electron microscopy (SEM) analysis, microprobe, residual stresses and phases, simulation / tests, summary of findings, preservation of evidence, formulation of one or more hypotheses, development of test methodologies, implementation of tests/collection of data, review of results and revision of hypotheses. Each time, the customer will be notified.

- First, the causes of a failure can be classified according to the phase of a product's life cycle in which they arise – design, materials processing, component manufacturing or service environment and operating conditions. Then two main areas of FA enable fast chip-level circuit isolation, circuit editing for quick diagnostic and problem-solving, helping bring forward semiconductor development: Physical inspection, represented by three important tools: SEM,

• emission microscopy and transmission electron microscopy (TEM).

• Electrical localisation, executed mainly with liquid crystal analysis (LCA), photo electron microscopy (PEM) and Focused Ion Beam (FIB).The package global localisation tool infra-red lock-in thermography (IR-LIT) became widely available in 2005 and is the most popular tool for global localisation for complex packages, such as system-in-package (SiP) and system-on-chip (SoC). Today the tool support for SoC development is X-ray CT, due to a significant resolution and speed improvement. FA has given and gives a continuous contribution to technological innovation in the whole history of semiconductor development.

Over the last few years, the increased complexity of devices has scaled the difficulty in performing FA. Higher integration has led to smaller geometry and better wire-to-cell ratios, thus increasing the complexity of the design. These changes have reduced the effectiveness of most of the current FA techniques; over the past few years, a variety of techniques and tools, such as electron-beam (E-beam) probers, FIB, enhanced imaging SEM to determine the defects at wafer level. All these tools improve FA capabilities, but at substantial cost, running into hundreds of thousands of dollars. Some other examples of new techniques are given below:

• A strategy was derived for FA in random logic devices (such as microprocessors and other VLSI chips) where the electrical scheme is not known. This strategy is based on the use of a test tool composed of an SEM allied to a voltage contrast, an exerciser, an image processing system and a control and data processing system [1].

• Three new FA techniques for ICs have been developed recently using localised photon probing with a scanning optical microscope (SOM) [2]. The first two are light-induced voltage alteration (LIVA) imaging techniques that *(i)* localise open-circuited and damaged junctions and *(ii)* image transistor logic states. The third technique uses the SOM to control logic states optically from the IC backside. LIVA images are produced by monitoring the voltage fluctuations of a constant current power supply as a laser beam is scanned over the IC. High selectivity for localising defects has been demonstrated using the LIVA approach. Application of the two LIVA-based techniques to backside FA has been demonstrated using an infrared laser source.

• It is critical to develop improved analysis techniques that are easier to use, less damaging, more sensitive and provide better spatial resolution. One example is 'passive' techniques, which are non-invasive, in the sense that the normal operation of the IC provides the information or energy being measured. Recently, dynamic photoelectric laser-stimulation techniques were applied to mixed-mode ICs, where the major difficulty is their considerable intrinsic sensitivity [3]. Indeed, the analogue circuitry is more sensitive than the digital circuitry since a slight change in an electrical parameter can trigger a functionality failure. This property limits the defect localisation because of the complex interpretation of the results: the laser-stimulation mapping. In this case, dynamic laser-stimulation mapping is coupled with photoelectric impact simulations run on a previously analysed structure. The goal is to predict and interpret the laser-sensitivity mapping and to isolate the defective areas in the analogue devices.

• A technique used for decapsulating the device for FA is the ultra-short-pulse laser-ablation-based backside sample-preparation method [4]. This technique is contactless, non-thermal, precise, repetitive and adapted to each type of material present in IC packages. However, it can create thermal contribution to technological innovation in the whole history of semiconductor development.

In the horizontal axis of Figure 1, applications drive the development of new technologies and its diversification. In the vertical axis, Moore's law predicts the exponential growth of number of transistors that can be placed inexpensively on an integrated chip. It is drives the rapid scaling down of gate width towards 22 nm and beyond. For future applications, higher value systems are expected with a form of SoC and SiP (System in Package), as result of the combination of the two. More Moore pushes the industry towards miniaturisation (left down of the Figure 1). More than Moore is the clear message that summarized the broad diversification in semiconductor applications. From analog/RF, passives, high voltage/power, sensors, to bio chips (the second horizontal line of Figure 1), the IC devices are exposing to harsher environment. The FA challenge is multiplied by the chip challenges (System-on-Chip SoC) and the package challenges (System-in-Package SiP). "*Assembly and packaging are limiting factors in both cost and performance for electronic systems"* states the latest version of the International Technology Roadmap for Semiconductors (ITRS). The resulting consequence: in next years, the FA will be extended to broader

aspects such as: design for analysis (or design for test), physical limit – tools for chip, tools for package, chip-package co-design, and organizational issues like FA cost, FA cycle time etc.

Chip sizes will stay constant over the next 10 years, but power will rise, accompanied by a drop in core voltage and no increase in allowed-junction temperature (except in harsh environments where operating temperatures will also increase). Pin count is expected to possibly double for the cost-performance market. While the thin gate oxide structures are very fragile, two new families of tools have immerged to facilitate probing such small components, Atomic Force Microscope (AFM) probe technology, and in-chamber scanning electron microscopy (SEM) or Focused Ion Beam (FIB) probe technology.

RIL (Resistive Interconnect Localisation) is a newer technique which can identify via anomalies functionally using induced thermal gradients to the metal but does not address how to uniformly inject the thermal energy required in the silicon to analyse timing design deficiencies and other defects.

With SIFT (Stimulus Induced Fault Testing), numerous stimuli will be used to identify speed, fault, and parametric differences in silicon. The heart of this technique [5] revolves around intentionally disturbing devices with external stimuli and comparing the test criteria to reference parts or timing/voltage sensitivities. Synchronous interfacing is possible to any tester without any wiring or program changes.

In paper [4], backside preparation examples are presented on a conventional DIL plastic package, a TSOP plastic package with an oversized silicon die, and on a DIL ceramic package.

Laser ablation is a recent pre-decapsulation technique, which is used for sample preparation in FA. This process works with speed and accuracy. These are key parameters for getting successful observation and defect localisation. This can be used to have a precise opening on the die. However, this technique can create thermal stresses to the device. In order to minimize this stress, paper [5] has investigated methods for controlling the thermal effect of the laser on the component. This paper presents the experimental setup and the study of an electrical artefact that influences the interpretation of the thermal data.

As new technologies in the electronic environment develop from 2D ICs to 3D complex packages, it becomes necessary to find new techniques to detect and localize the different kinds of failures. A solution to localize defects for SiP devices is to measure the magnetic field that is generated by the current owing through the device, with a magnetic microscope (Magma C20) and comparing it with several simulated faults in order to choose the most probable one [6].

The new FA requirements put a high demand on the inspection tools with regard to accuracy and resolution. The resolution of single-beam FIB instruments is not sufficient anymore to deal with the necessary accuracy. To overcome this problem, the FIB tool must be combined with a high-resolution SEM that is used to monitor the FIB work on a nanometre scale. These integrated CrossBeam tools [7] enable the observation and direct control of the FIB operation in real time. The CrossBeam tools combine the imaging and analytical capabilities of a high-resolution field emission SEM (FESEM) with a high-performance FIB column into one integrated instrument. In the case of the CrossBeam tool, the final lens of the FESEM is designed as a magnetic/electrostatic compound lens. This layout has the advantage of no magnetic field interfering with the ion beam, and the FESEM can be operated at nanometre resolution during the ion milling process. This layout allows full control over the total process and gives an excellent endpoint detection and cut localization for defect review and FA [7].

5. FAILURE MODES

Electronic components have a wide range of failure modes. These can be classified in various ways, such as by time or cause. Failures can be externally utility generated, *in-situ* facility or locally generated by other nearby equipment or machinery, or internally generated from other related components in the circuitry. They can be caused by excess temperature, excess current or voltage, ionizing radiation, mechanical shock, stress or impact, parasitic structures, and many other causes. They can happen in an instant or take time to manifest. They can happen in storage, on manufacturing, in handling, packaging, shipping, installation, or during maintenance. In some electronic semiconductor devices, such as LEDs, problems in the device package may cause failures due to contamination, mechanical stress of the device or open or short circuits.

Failures most commonly occur at near the beginning and near the ending of the lifetime of the parts, resulting in the bathtub curve graph of failure rates. Burn-in procedures are used to detect early failures.

Analysis of the statistical properties of failures can give guidance in designs to establish a given level of reliability. For example, power-handling may be greatly derated to obtain adequate service life; a part intended to run for years has different reliability requirements than a part intended to run for 6 months or a year.

A sudden fail-open fault in an inductive circuit can cause multiple secondary failures. A broken metallization [printed circuit board (PCBA)] may cause secondary overvoltage damage. Thermal pads, vias, and metalized plans can add capacitance and discharge paths to ground. Thermal runaway can cause sudden failures including melting, fire or explosions. Paint can add high resistance to paths needing electrical continuity. Any fault effects can be cumulative or systemic where circuits feed other circuits.

6. FAILURE MECHANISMS

From a technical perspective, failure can be defined as the cessation of function or usefulness. FA is the process of investigating such a failure. Basically, FA is analysing the failure modes (FMo) with the aim to identify the failure mechanisms, by using optical, electrical, physical, and chemical analysis techniques.

Reliability is built into the device at the design and manufacturing process stages. In most practical cases, the final damage quite rarely reveals a direct physical FM; often the original cause (or complete scenario of failure) is hidden by secondary post damage processes. On the other side, it is impossible to eradicate failures during the manufacturing process and at field use. Therefore, FA must be performed to provide timely information to prevent the recurrence of similar failures. Or, wafer fabrication and assembly process involves numerous steps using various types of materials. This, combined with the fact that devices are used in a variety of environments, requires a wide range of knowledge about the design and manufacturing processes. This explains why FA of semiconductor device is becoming increasingly difficult as VLSI technology evolves toward smaller features and semiconductor device structures become more complex. Since it is usually not possible to repair faulty component devices in a VLSI, each device in a chip can become a single point of failure unless some redundancy is introduced. Therefore, VLSIs have to be designed based on the characteristics of worst devices rather than those of average devices. Even if a chip is equipped with some redundant devices, today's scale of integration is becoming so high, that the yield requirement is still very severe. The final chip yield is governed by the device yield.

CONCLUSION

Going further from microsystems, another challenge for FA comes from a new domain, called nanotechnology. Here everything is new and the FMs for nanomaterials, which are different from those of the same materials at micro level, have to be studied. Supplementary issues are induced by using organic materials, which is a new trend in this field. Also, at nano level, new techniques for FA have to be created [8]. As one can see, nano-reliability (studying the reliability of nano-devices) offers a huge range of subjects for FA. The near future will show an important step forward in this field.

In conclusion, it is both easy and difficult to predict the future evolution of FA. Easy, because everyone working in this domain can see the current trend. Now the FA is still in a 'romantic' period, with fabulous pictures or smart figures smashing the customers, convinced by such a 'scientific' approach. Seldom, these users of electronic components do understand the essence of the FA procedure, because the logic is frequently missing. But this situation is only a temporary one. Very soon, the procedures for executing FA will be stabilized and standardized, allowing to any user of an electronic component to verify the reliability of the purchased product [9].

But it is also difficult to predict the evolution of FA, because the continuous progress in microelectronics and microtechnology makes almost impossible to foresee with maximum accuracy the types of electronic components that will be most successful on the market. And the FA must serve this development, being one step ahead and furnishing to the manufacturers the necessary tools for their researches. However, with sufficiently high probability one may say that the nanodevices (or even nanosystems) will become a reality in the next five years, so we have to be prepared to go deeper inside the matter, with more and more expensive investigation tools.

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