MICRO- AND NANO-ENGINEERING OF SEMICONDUCTOR COMPOUNDS AND METAL STRUCTURES BASED ON ELECTROCHEMICAL TECHNOLOGIES

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Summary of the synthesis work for the title of Doctor Habilitat in Physics, elaborated on the basis of published scientific papers

Abstract. This paper aims to address the challenges of micro- and nano-engineering semiconductor compounds and fabricating metal-semiconductor nanocomposite materials by developing theoretical concepts for the application of electrochemical nanostructuring technologies to semiconductor substrates. It includes identifying the technological conditions for controlled electrochemical etching to create nanostructured semiconductor templates with wide bandgaps, such as III-V semiconductors (InP, GaAs, GaN) and II-VI compounds (CdSe, ZnSe, $Zn_xCd_{1-x}S$). The study also demonstrates the conditions for electrochemical metal deposition in porous semiconductor templates and investigates the laws and mechanisms of metal deposition depending on the composition of the semiconductor substrates and current pulse parameters. Additionally, the paper addresses the conditions for electrochemical etching of semiconductor substrates to produce nanowire networks with directed alignment to the substrate surface, instead of merely producing porous layers. A comprehensive investigation of the properties of the developed nanostructures and materials is proposed to demonstrate their applicability in nanoelectronic, optoelectronic, and photonic devices.

Keywords: Wide bandgap semiconductors, Crystallographically oriented pores, Current line oriented pores, Pore growth direction, Hopping electrodeposition, Anomalous retroreflection, IR photodetector, Integrated photonic lenses, Magnetic anisotropy, Hybrid core-shell structures, Hydrophilic/hydrophobic properties, Varicap.

DOI **10.56082/annalsarsciphyschem.2024.1.85**

1. Introduction. Motivation of the study

Starting with the rapid development of nanotechnology in the 1990s, a wide range of porous materials were developed. The discovery of macroporous silicon by Lehmann and Föll over thirty years ago generated significant interest [1]. Nowadays, several well-studied self-ordered porous materials are used in various fields, including: (i) porous alumina developed by Masuda and Fukuda in 1995 [2];

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(ii) TiO_2 nanotubes introduced by Macak and colleagues in 2007 [3]; and (iii) self-ordered porous III-V semiconductor compounds [4–8].

However, despite the versatility of porous alumina oxide in introducing self-ordering, its applicability as a porous template is limited because it requires filling with other materials and subsequent removal due to its dielectric behavior, resulting in a passive role in nanofabrication processes. In comparison, TiO_2 nanotube-based templates have attracted significant attention in research and are considered as a semiconductor nanoarchitectures with potential for a variety of applications due to their unique structural, optical, and electronic properties, non-toxicity, corrosion resistance, accessibility, biocompatibility, high photocatalytic characteristics, photostability, and more. Although TiO_2 is classified as a semiconductor material, its electrical conductivity is relatively low. Therefore, semiconductor porous structures with controlled conductivity are of significant interest. Porous materials from the III-V group are ideal candidates to fill this gap. Notable contributions to the controlled nanostructuring of these materials have been made by the research groups of Prof. H. Föll, Prof. I. Tiginyanu, and Prof. P. Schmuki.

The authors of Ref. [6] have focused their study on the formation of pores in III-V semiconductor compounds, emphasizing the influence of electrochemical parameters on the ordering and types of pores that can be obtained. It was highlighted how various parameters like crystallographic orientation of semiconductor substrates, type of electrolyte could affect pore morphology [9, 10], but systematic data on the controlled formation of pores with different shapes, morphologies, and compositions in semiconductor compounds are still lacking. While their findings provide valuable insights into the initial stages of pore formation, there is a clear need for further research to develop a comprehensive understanding of how to precisely control pore characteristics in these materials. As a result, the problem of engineering porous semiconductor compounds at the micro- and nano-metric scale is of significant importance in the design of various electronic devices and systems. This gap in the literature points to the importance of more detailed studies that can explore and establish methodologies for achieving desired pore structures, which could significantly advance the field of semiconductor technology and its applications. The ability to control and manipulate the electronic properties of these semiconductor nanotemplates would be particularly advantageous for advancements in electronics, photonics, and sensor technologies.

Engineering of pores in semiconductor compounds using electrochemical techniques provides numerous benefits for device design. Furthermore, these methods enable the controlled integration of other materials into porous semiconductor compounds, facilitating the creation of hybrid or functionalized

devices with potential applications in electronics, photonics, optoelectronics, and energy storage.

The aim of the synthesis work is to develop theoretical concepts and to develop technological approaches for micro- and nano-engineering of porous semiconductor compounds and metallic nanostructures by electrochemical methods for multifunctional applications.

Achieving the goal is conditioned by the achievement of the following specific **objectives**:

- Identification of the technological conditions of the electrochemical etching to obtain templates based on wide bandgap semiconductors;
- Elaboration of concepts with further experimental demonstration for the engineering of the morphology of porous layers in semiconductor compounds by electrochemical etching;
- Comparative analysis of the nanostructuring of III-V (InP, GaAs, GaN) and II-VI semiconductor compounds (CdSe, ZnSe, $Zn_xCd_{1-x}S$);
- Investigation of the electrochemical pulse deposition of metal on porous semiconducting layers for the identification of legalities and the development of the deposition mechanism;
- Development and optimization of electrochemical technologies for switching from porous layers to arrays of nanowires with controlled alignment with respect to the surface of the substrate;
- Properties investigation of the elaborated nanostructures in order to demonstrate their applicability in micro- and nano-devices in electronics, optoelectronics, photonics, ferromagnetism.

The detailed description of the used semiconductor substrates, investigated electrolytes and the schematic representation of the technological set-up is reflected in the chapter 5 of the author's monograph [11].

The novelty and scientific originality of the synthesis work consists in:

- Porous templates based on wide bandgap materials (GaN, ZnCdS) and micro-nano-structures (ZnO), perspective for applications in the visible range of the spectrum, were fabricated;
- Electrochemical technological approaches have been developed to control the pore direction propagation in depth, resulting in 3D structures formed as a result of the transition from current line oriented (CLO) to crystallographically oriented (CO) pores, or due to non-uniform doping in HVPE grown GaN substrates, as well as parallel to the surface of InP or ZnSe crystals by applying specially designed photolithographic masks;

- The "hopping electrodeposition" mechanism was developed and demonstrated, which allows the deposition of a monolayer of Au nanodots on porous semiconductor compounds, regardless of morphology;
- For the first time, the "abnormal" retroreflection of light on ultra-porous layers based on InP and GaAs semiconductor compounds was demonstrated;
- Optimization of the technological parameters of anodization allowed the fabrication of semiconductor nanowire arrays by electrochemical etching of InP, GaAs and ZnTe semiconductor crystals. The use of GaAs crystals with different crystallographic orientation allowed obtaining networks of nanowires tilted (100), perpendicular (111)B and predominantly parallel (001) to the substrate surface;
- For the first time, a cost-effective and original approach was proposed to estimate the electrical conductivity in InP semiconductor nanostructures with different thicknesses, by pulsed electrochemical metal deposition. The given approach has also been shown to be effective for highlighting non-uniform doping during HVPE growth in GaN substrates. Complementarily, non-uniform doping was also demonstrated by electrochemical etching of GaN (HVPE) substrates;
- Through contact angle analysis, it has been demonstrated that the engineering of semiconductor surfaces by electrochemical methods (electrochemical etching and/or electrochemical deposition) allows the controlled switching of hydrophilic/hydrophobic properties.

The main scientific results submitted for defense:

- The "hopping electrodeposition" mechanism for the self-assembly of Au nanodots in monolayers is governed by the formation of the Schottky barrier at the interface of the semiconductor substrate with Au nanodots with diameters around 20 nm, confirmed by means of topographic imaging and current mapping measurements.
- Electrochemical methods allow the design and control of nanoscale porous structures in semiconductor and metallic materials.
- Joining the porous semiconductors and metallic structures on a nanometric scale by electrochemical methods allows the creation of hybrid materials with unique properties, having significant implications in the development of advanced devices in the field of electronics, optoelectronics and photonics.
- The concepts of the integration of electrochemical etching with patterned photolithographic masks containing opening holes provides an innovative approach for fabrication of porous domains with separate entrances for fluid manipulation at the micro- and nanoscale.
- Choosing the optimal electrochemical parameters (applied voltage, nature of the electrolyte and its concentration) offers the possibility of obtaining an

enormous amount of semiconductor nanowires (InP, ZnTe, GaAs) connected to the bulk semiconductor substrate.
- The anomalous retroreflection demonstrated in nanoporous InP and GaAs materials with mesh-like morphology that strongly absorb in the visible range occurs in a narrow solid angle along with a diffuse specular reflection for all angles of incidence.
- CLO pores are characteristic of both III-V (except GaAs) and II-VI semiconductor compounds, while CO pores have only been observed in III-V semiconductor compounds.
- The presence of only CO pores in the anodization process of GaAs crystals, offers additional possibilities of aligning the nanowires obtained by electrochemical etching, by choosing the crystallographic orientation of the bulk GaAs substrate.

2. Wide bandgap semiconductor nanotemplates (GaN, $Zn_xCd_{1-x}S$, ZnO)

In this chapter, the results of wide bandgap semiconductor compounds nanostructuring via electrochemical etching of: (i) HVPE grown GaN substrates; (ii) $Zn_xCd_{1-x}S$ solid solutions; (iii) ZnO crystals were systematized.

The advantages of HVPE for GaN crystal growth compared to other methods, such as sodium flux growth, ammonothermal growth, and metal-organic chemical vapor deposition (MOCVD) on sapphire, Si, or SiC substrates, are highlighted [12]. These advantages include higher growth rates, reduced impurity presence, and fewer defects that hinder material use in device applications. MOCVD technology limits the production of porous GaN layers to depths of 2–4 μm. Additionally, epitaxial layers obtained by this method suffer from internal stresses and defects due to differences in lattice parameters and thermal expansion coefficients between the layer material and substrate.

In the work [13], it was demonstrated that electrochemical etching allows the highlighting of self-organized three-dimensional nanostructured architectures, which were attributed to the spatial modulation of electrical conductivity generated during the HVPE growth of GaN substrates acquired from SAINT-GOBAIN Crystals. The results of a more detailed investigation of the modulation of electrical conductivity and lattice distortions in etched HVPE GaN substrates are presented in the work [14]. It should be mentioned, that the electrochemical etching allowed to investigate the uniformity of the doping of the HVPE grown GaN substrate in bulk (see Figure 1d), while with Kelvin probe force microscopy (KPFM) only the surface can be investigated (see Figure 1b). It has been shown that the porosity of the GaN layers in the multilayer porous structure is controlled by several technological parameters such as: composition and the concentration of the electrolyte, as well as the applied anodization potential [15].

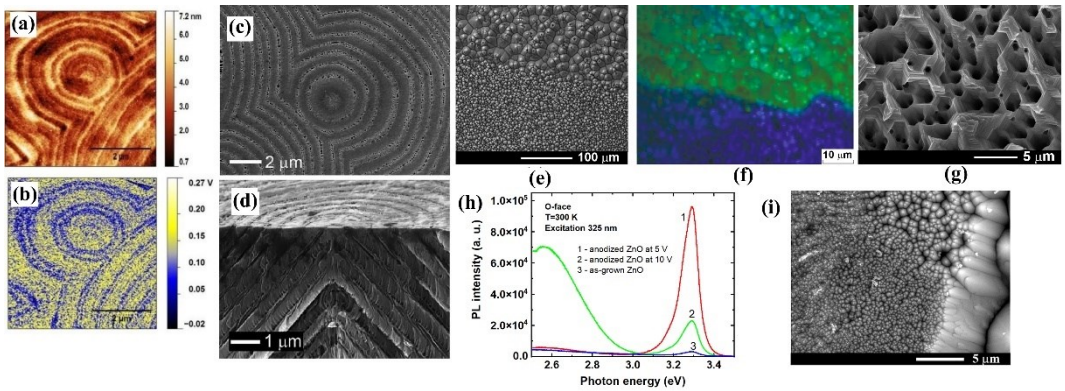

Fig. 1. a. AFM image of the surface of a HVPE grown GaN substrate. **b.** KPFM image of the surface shown in (a). SEM images of the GaN sample subjected to electrochemical etching: top view (**c**) and cross-sectional view (**d**) of the N surface [13]. **e.** SEM image of the morphology of an *n*-ZnO crystal anodized on the O-face in 5% HCl electrolyte for 2 min at the applied potential of 5 V (small pyramids) and 10 V (large pyramids). **f.** CL image of the small and large pyramids from image (a). **g.** SEM image of *n*-ZnO anodized on Zn-face at 10 V, showing formation of inverse pyramids. **h.** PL spectra measured at room temperature from O-face of ZnO crystal before anodization (curve 3) and after anodization at 5 V (curve 1) and 10 V (curve 2). **i.** Top-view SEM images of anodized ZnO crystal on O-face in HNO_3 electrolyte at applied potential of 8 V [16, 17].

As concern the uniformity of porous nanotemplates, different porous morphologies produced by deep anodization of 300 μm thick HVPE grown GaN substrates (MTI-corporation, USA) with respect to N or Ga face were demonstrated in the paper [18]. Porous structures in the form of pyramids were formed on the N face, while homogeneous porous templates with pores oriented perpendicular to the wafer surface are generated at a depth of up to 50 μm on the Ga face. These characteristics are explained by the variations in electrical conductivity along the wafer resulting from the growth mechanisms of the HVPE technology. Beside this, the possibilities of producing porous GaN structures in neutral NaCl electrolyte were demonstrated. HR-STEM analysis of porous GaN structure demonstrates the preservation of the high-quality wurtzite crystalline phase of the material [18].

The section on micro- and nano-structuring of ZnO crystals discusses results of anodization on either the O-face or Zn-face of ZnO crystals, as well as the photoluminescence and cathodoluminescence properties of nanostructured layers [16]. The research highlighted the capability to selectively fabricate ZnO micro- and nanostructures with diverse shapes via anodization on various surfaces of a ZnO crystal. On the O-face, the microstructures with a pyramidal shape are obtained (see Figure 1e), while the Zn-face resulted in formation of inverted pyramids or tunnels as can be seen in Figure 1g. Moreover, we revealed that the size of these microstructures can be controlled by varying the applied potential during anodization and by choosing the appropriate electrolyte for the process [16, 17].

The cathodoluminescence (CL) and photoluminescence (PL) study revealed a significant dependence of the emission properties on the dimensions of ZnO micro- and nanostructures. It was demonstrated that blue emission is dominant in regions with small pyramids obtained at anodization potential of 5 V having a base of 1–5 μm (bottom of Figure 1f), while green emission predominates in areas with large pyramids obtained at 10 V (top of Figure 1f). The morphology obtained through anodization on the Zn-face differs significantly, resulting in hexagonal pits (inverted pyramids), as shown in Figure 1g. It is noteworthy that the formation of pyramidal structures on the O-face and stepped hexagonal pits on the Zn-face has also been observed on ZnO and GaN thin films during wet chemical etching [19, 20]. Additionally, a novel asymmetric morphology featuring 1 μm hexagonal pyramids with a Zn-terminated bottom surface has been achieved using microwave synthesis [21].

Another significant study [17] was conducted to elucidate the influence of the type of electrolytes and the applied potential during the anodization process of ZnO crystals on the resulting morphology. Anodization of the O-face was performed in three different aqueous solutions: 5% HCl, 1M HNO_3, and $K_2Cr_2O_7$ (1g $K_2Cr_2O_7$:10 ml H_2SO_4:100 ml H_2O). Each electrolyte produced different morphologies under the same applied potential. For the first time, a columnar morphology reaching a length of 5 μm, instead of hexagonal pyramids was reported in the HNO_3 electrolyte (Figure 1i). The morphology appeared completely different after anodization in $K_2Cr_2O_7$ electrolyte, showing a sponge-like structure [17].

At the same time, $Zn_xCd_{1-x}S$ solid solution crystals with composition in the range of $0.4 \leqslant x \leqslant 0.6$, have been shown to be a promising material for the fabrication of nanoporous templates with pore diameters up to 30 nm and 20 nm wall thickness via electrochemical etching [22, 23, 24]. The anodization of samples with the composition $x>0.6$ is limited by the low electrical conductivity inherent in these materials [25].

The final paragraph of this chapter provides a comparative analysis of the anodization of III-V semiconductor compounds (InP, GaAs, GaN) and II-VI compounds (CdSe, ZnSe, ZnxCd1-xS) [26], it was established that the absence of CO pores in II-VI semiconductor compounds and the possibility of their growth in III-V semiconductor compounds is explained by the degree of ionicity of the chemical bonds. The CLO pores grow in almost all semiconductor compounds, except GaAs [27, 28]. However, in II–VI semiconductor compounds, CLO pores grow over a wide range of applied potential during electrochemical etching, while in III–V compounds they grow only at high values of the applied potential. The absence of CLO pores in GaAs requires further investigation.

In the paper [28], was demonstrated the possibility of 3D structures obtaining representing Bragg-like structures, composed from parallel or undulated layers with different degree of porosity due to the presence of CO and CLO pores, as well as the optimization of electrochemical etching parameters.

3. Engineering of porous semiconductor compounds and metallic structures by electrochemical methods

Chapter two is devoted to the engineering of porous semiconductor compounds and metal structures through electrochemical methods. The first paragraph elaborates on the technology for fabrication of templates with pores parallel to the surface of *n*-InP or *n*-ZnSe substrates [26, 29]. It is important to note that the electrochemical nanostructuring of InP semiconductor compound was also developed and demonstrated in an environmentally friendly neutral electrolyte NaCl [30–32]. Electrochemical porosification of semiconductor compounds combined with the application of special masks brought to light a variety of fascinating morphologies, including formation of networks of pores oriented parallel to the top surface of the semiconductor substrate and of porous domains excluding pore percolation between them. The exploration includes the possibility of obtaining various pore topologies by design, combining anodization with photolithographic techniques, which allow precise control over the self-organization of the pores [37]. The flexibility of this approach is further demonstrated by applying a photoresist (PhR) mask design with specific holes (see Figure 2), considering the hole diameter and the distance of the hole from the edge of the PhR mask [17].

In continuation, it was shown that an alternative and cost-effective technology for fabrication of one dimensional nanostructures is electrochemical etching of bulk semiconductor crystals. This method not only proves its efficiency but also demonstrates the ability to transition from porous structures to networks of *n*-InP nanowires, nanobelts, and nanomembranes [33] and *p*-ZnTe nanowires [34]. The electrical and optical properties of InP nanobelts have been shown to differ from those of InP nanowires, with experimental demonstration revealed in paper [53]. Such advancements highlight its potential in various applications, including electronics, photonics, and sensing, where precise control over nanostructure morphology is crucial. The obtaining of semiconductor nanowires by anodization on *n*-GaAs crystals in nitric acid electrolyte, with the possibility of controlling the orientation of the nanowires with respect to the substrate surface was demonstrated [11, 28, 35, 36]. As a result, tilted to the surface GaAs nanowires were obtained using substrates with (100) crystallographic orientation, perpendicular to the surface nanowires for (111)B orientation and predominantly parallel to the substrate surface nanowires formed in the case of crystals with (001) orientation. This capability enhances the precision and versatility of nanostructure fabrication,

making it possible to tailor the properties and orientation of nanowires for specific applications in advanced electronic and photonic devices.

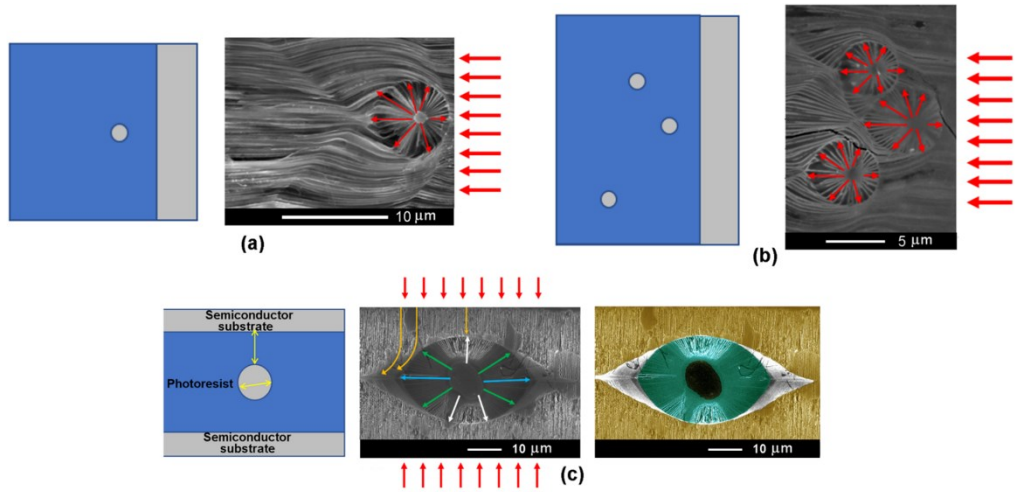

Fig. 2. Schematic design (left) and (right) SEM image of anodized *n*-InP from one side using PhR masks with one (**a**) and three (**b**) open holes in the PhR. **c.** Schematic design of the mask (left side), SEM image of anodized InP from two opposite PhR edges using PhR mask with one open hole in the PhR leading to the "eye-like" porous structure (center part), and NanoArt visualization of the SEM image (right side) [17].

The third paragraph details the pulsed electrochemical deposition of metallic nanoparticles in porous semiconductor compounds. It is important to mention the necessity of removing the porous surface layer [37], which consists of crystallographically oriented pores, and adjusting the pulse parameters to ensure uniform deposition within the porous layer [38], resulting in formation of metal nanotubes embedded in a semiconductor shell. To explore the formation of hybrid metal-semiconductor nanostructures, it has been demonstrated that the huge surface area of porous *n*-GaP and *n*-InP structures can be covered with a self-assembled monolayer of Au nanodots using pulsed electrochemical deposition (Figure 3a,b) [39]. The so-called "hopping electrodeposition" mechanism was proposed to explain the deposition of a monolayer of gold nanodots on porous semiconductor structures (see Figure 3c).

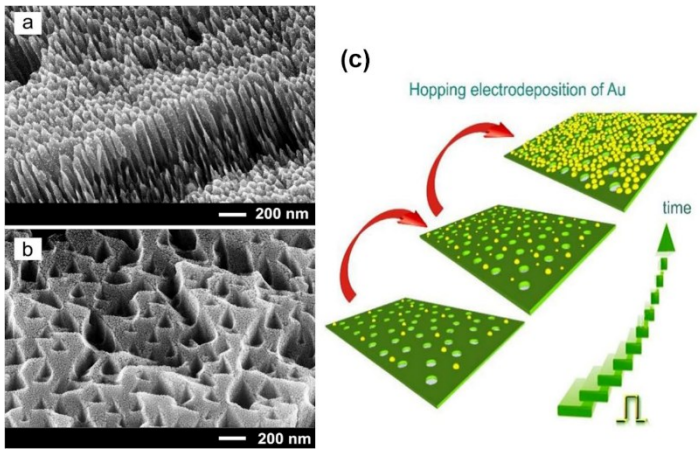

Fig. 3. SEM images of porous *n*-GaP after electrochemical deposition of Au dots for 5 s (**a**) and 100 s (**b**) and schematic illustration of the "hopping electrodeposition" mechanism (**c**) [39].

Accordingly, to this mechanism it was established that after nucleation, each nanodot grows up to a critical diameter of approximately 20 nm, determined by the Schottky barrier height at the interface with the semiconductor substrate. This value corroborates previously published data for the electrodeposition of Pt on bulk *n*-InP wafers, providing evidence that the Schottky barrier height depends on the size of the Pt dots [40]. As the diameter of the metal dots increases, the surface barrier height rapidly rises to the Mott-Schottky limit of 1.1 eV, reached at a gold nanodot diameter of approximately 23 nm. Subsequently, the formation of a new metal nanoparticle is initiated, and the deposition process continues until the entire surface exposed to the electrolyte is covered by a self-assembled monolayer of gold nanodots. The formation of the Schottky barrier at the interface of Au nanodot and semiconductor surface was demonstrated in study [41], where current mapping topographic imaging using point-contact microscopy was employed to experimentally show the barrier at the metal-semiconductor interface.

Additionally, the paragraph includes a comparative study using electrochemical impedance spectroscopy (EIS) on porous *n*-GaN and *n*-GaP structures, both with and without metal layers obtained through pulse electrodeposition [42]. This comparative study provides insights into the electrical characteristics and stability of the nanostructures, which are vital for their performance in electronic and catalytic applications.

In the paper [43] an innovative method for estimation of the electrical conductivity of 1D and 2D semiconductor nanostructures using pulsed electrochemical deposition of metal nanodots was proposed and demonstrated. This approach is based on the previously discussed "hopping electrodeposition" mechanism [39], and takes into account the geometric dimensions of the InP nanostructures. This approach offers a new way to assess conductivity, providing important insights for

advancements in nanotechnology. This statement is confirmed by the results of Au nanodots electrodeposition concomitantly on 10 nm thick nanowall nanostructures, nanowires with 50 nm diameter and 2 nm thick InP nanobelts, as well as on bulk *n*-InP substrate. Comparison of the electrodeposition of 20 nm diameter Au nanodots on InP nanowires and on bulk InP suggests that the electrical conductivity of nanowires is similar to that of bulk crystals. At the same time, the comparison of the electrochemical coating of Au nanodots on nanowires and nanowalls indicates a much lower conductivity of nanowalls compared to that of nanowires, and the absence of deposition of Au nanodots on InP nanobelts demonstrates that there are no free charge carriers in nanobelts with a thickness of several nanometers. Based on these findings, it was demonstrated that the hopping deposition of nanodots, which depends on the geometrical transverse dimensions of the semiconductor nanostructures, can effectively deposit Au nanodots along specific lines [44]. Electrochemical deposition of gold, governed by the "hopping electrodeposition" mechanism, has also been used to demonstrate the modulation of electrical conductivity in HVPE-grown GaN crystals [45].

The final paragraph explores the possibility of controlling the hydrophobic/ hydrophilic properties of semiconductor structures through anodization or electrochemical metal deposition on bulk or porous semiconductor substrates. This investigation is significant for applications in surface chemistry and material science, where surface wettability plays a crucial role. It was demonstrated that the anodization and electroplating of metals on the bulk or porous semiconductor layers have a great impact upon the wetting properties of surfaces leading to pronounced hydrophilic or hydrophobic behavior [17, 46, 47]. It was shown that the morphology of pores, tilted or perpendicular to the surface, play an important role in switching from the hydrophobic to hydrophilic properties. The ability to modulate these properties opens up possibilities for creating advanced materials with tailored surface characteristics, suitable for a wide range of applications, including biomedical devices, microfluidics, water-repellent coatings, and advanced filtration systems.

4. Retroreflection of light in porous semiconductor compounds (InP, GaAs). Photonic nanostructures (GaN, GaP, ZnSe)

Chapter three is dedicated to the study of light retroreflection in porous semiconductor compounds and the development of photonic nanostructures. In the paper [48], anomalous retroreflection has been discovered in 2011 for a fishnet nanoporous *n*-InP semiconductor material strongly absorbing in the visible range. The study revealed that the retroreflection occurs in a narrow solid angle along with a diffusive specular reflection for all angles of incidence. Subsequently, the investigation of the retroreflection and scattering properties of the mesh-like porous

InP was continued, not only in the spectral range of interband optical transitions where multiple scattering is inhibited by strong absorption, but also in the infrared spectral region where this material is transparent. The experimental measurements demonstrated systematic manifestation of retroreflection in scattering diagrams for the wavelengths 531 nm and 654 nm, where the optical absorption (interband) is high, $\alpha=1.3\times10^5$ cm^{-1} and respectively $\alpha=0.6\times10^5$ cm^{-1} [49]. Backscattering is more pronounced for *p*-polarized compared to *s*-polarized radiation, it shows an apparent tendency to increase when the angle of incidence moves from normal to oblique incidence (compare the data for 20° and 40°) and vanishes for wavelengths corresponding to low intrinsic absorption (1064 versus 532 nm (Figure 4) [50].

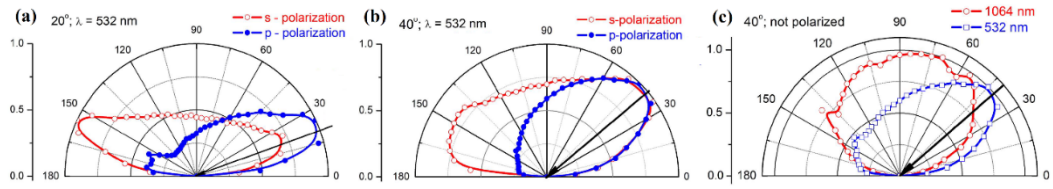

Fig. 4. Angular dependent scattering diagram of a nanoporous InP sample for different angles of incident light (20° (**a**) and 40°(**b,c**)) for *s*- and *p*-polarization, and different wavelengths corresponding to low (1064 nm) and high (532 nm) intrinsic interband absorption in InP [50].

Following extensive research on the experimental observation of retroreflection in porous *n*-InP layers [48–51], the phenomenon was later experimentally confirmed in porous *n*-GaAs layers [52, 53]. Additionally, a mathematical model for calculation of the scattered radiation by a highly absorbing porous medium with dark modes was proposed [54].

The third paragraph discusses the development of Bragg reflectors based on multilayer GaN structures. The potential to create multilayer porous structures in *n*-GaN grown by both HVPE and Metal-Organic Chemical Vapor Deposition (MOCVD) using electrochemical etching has been demonstrated. In HVPE-grown GaN, these multilayer porous structures form due to uncontrolled self-modulation of doping during crystal growth [13]. In contrast, MOCVD-grown GaN allows for the fabrication of multilayer porous structures with controlled spatial design [55]. Optimization of the electrochemical etching conditions in oxalic acid and KOH electrolytes has enabled the production of high-quality multilayer porous GaN structures. The feasibility of these structures for designing Bragg reflectors or other photonic elements was confirmed through micro-reflectivity measurements, transfer matrix analysis, and simulations using a method developed to calculate optical reflection spectra [55].

In the final paragraph of this chapter, the prospect of developing new focusing elements and beam splitters based on GaP/Pt or ZnSe/Pt nanostructures, for applications in the visible region of the spectrum, was demonstrated [29, 56]. The

photonic properties of porous structures metallized with nanotubes were found to be determined by both the spatial distribution of the nanopores or nanotubes and their geometrical dimensions, as well as the composition of the semiconductor material used. By decreasing the pore diameter or inner diameter of the nanotubes by a factor of two, the purpose of the photonic slab can be changed from a focusing lens to a beam splitter.

5. Applications of elaborated semiconductor nanostructures

In the last chapter, some applications of semiconductor nanostructures fabricated by electrochemical methods have been demonstrated. An important compartment of semiconductor compound engineering for nano-micro-electronics was demonstrated by the development of varicap device based on GaP/Pt nanostructures with a record capacitance density variation of 6×10^{-3} pF·V^{-1} per 1 μm^2 of surface area [56, 57]. It is worth mentioning that the value can be further increased by using porous GaP templates with a pore depth of 300 μm [58] compared to 70 μm [56].

The feasibility of applying the developed nanostructures as photodetectors in IR region was demonstrated based on an ultra-thin (10 nm) InP nanowall [59], which demonstrated a photoresponse R=1.3 A·W^{-1} and detectivity D=1.28×10^{10} cm·Hz$^{1/2}$·W^{-1}, as well as GaAs photodetector (single nanowire) with values R=100 mA·W^{-1} and D=1.2×10^{9} cm·Hz$^{1/2}$·W^{-1} at optical excitation power P_{exc}=800 mW·cm^{-2} [35, 58].

It was demonstrated the possibility of hybrid core-shell nanowires networks fabrication based on GaAs-Fe [36] or GaAs-NiFe [60,61], with Ni contents of 65%, 80% and 100%, both on planar GaAs substrates and on nanowire arrays fabricated by anodization of n-GaAs substrates with (111)B and (001) crystallographic orientation, which revealed a magnetic anisotropy of coercivity and remanence ratio. The optimization of Ni deposition process in porous InP layers was also carried out [37]. The magnetic parameters for both Fe and NiFe coatings were found to be more advantageous for coaxial core-shell structures compared to planar structures. At the same time, these parameters are higher for the configuration with the magnetic field oriented in the radial direction of the coaxial core-shell structures compared to the orientation along the axis of the nanowires. It was determined that by controlling the deposition duration, resulting in a larger thickness of the Fe coating on GaAs nanowire arrays, is assured an increase in coercivity and remanence ratio from 62 to 284 Oe and from 0.35 to 0.70 respectively (see Figure 5a-c) [61]. Controlling the geometrical shape of pores or semiconductor nanowires, which are used as templates for the deposition of metals with magnetic properties by means of the "hopping electrodeposition" mechanism, allows obtaining hybrid core-shell structures with triangular, square or round geometries, by forming a thin metal layer inside the pores or around the nanowires (Figure 5d,e) [17, 28].

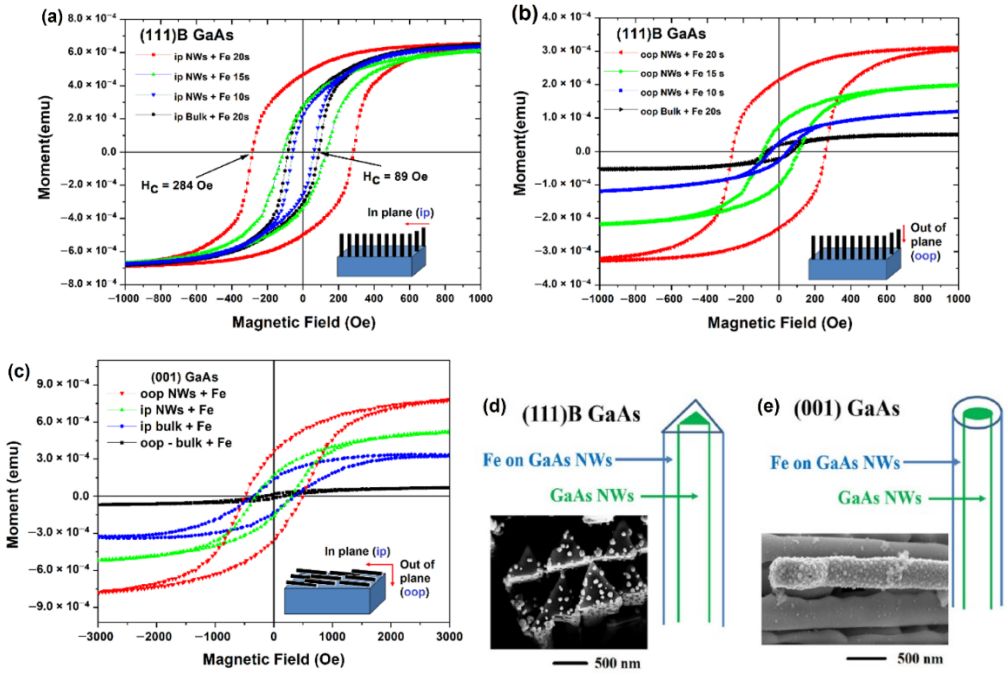

Fig. 5. Hysteresis loops measured in "in-plane" (**a,c**) and "out-of-plane" (**b,c**) configurations on a nanowires array fabricated on GaAs (111)B substrates (**a,b**) and (001) in (**c**) compared with measured planar substrates coated with a Fe film [36]. (**d,e**) Schematic representation and experimental demonstration of nanowires formation with different geometric shape and resulting metal coating [28].

The formation of core-shell structures has also been demonstrated through the Atomic Layer Deposition (ALD) method applied to GaAs nanowire networks. This method allows for precise and uniform coating of the nanowires, resulting in well-defined core-shell architectures that enhance the material properties and enable various advanced applications [62, 63].

A two-step technological approach for Ga_2O_3 nanowire arrays functionalization with Au nanodots by pulsed electrochemical deposition has been proposed and demonstrated, with the high electrical resistance of the nanowire arrays being one of the critical factors in this process. The first technological step consists in the deposition of Au nanodots on GaAs nanowires, and the second step involves thermal treatment, during which the oxidation of GaAs nanowires takes place [38]. Thus, additional technological steps of sensitization and activation of the gallium oxide surface were avoided, which could lead to contamination and the formation of unwanted residues.

It has been demonstrated that the elaborated "hopping electrodeposition" mechanism provides an efficient platform for functionalization and modification of nanostructured surfaces, which enables precise control over the process parameters.

It has been shown that using pulses can avoid some of the adverse effects associated with continuous deposition, such as formation of nonuniform layers, diffusion-limited phenomena, and supersaturation. As a result, the possibility of gold nanodots deposition with controlled density on various nano-micro-structured semiconductor substrates such as: (i) hollow GaN microtetrapods arrays from aero-GaN [45], (ii) porous microdomains with a controlled design produced by anodization of *n*-InP substrates and (iii) complex microdomains composed of strips with alternating electrical conduction based on HVPE grown *n*-GaN substrates was demonstrated [45]. The self-assembled gold nanodots can serve as catalyst nucleation sites for growth of nanowires with different chemical compositions to form complex 3D hybrid micro-nano-architectures promising for photocatalytic applications [64, 65].

Conclusions

Semiconductor templates based on wide bandgap materials, promising for applications in the visible range of the spectrum, have been fabricated by electrochemical etching of *n*-GaN (HVPE) or ZnCdS crystals possessing a deepness of porous layer of 70 μm, in contrast to 2 – 4 μm for MOCVD grown GaN layers. It has been demonstrated the obtaining by electrochemical etching of multilayer porous structures based on GaN grown by the HVPE method, due to the uncontrolled self-modulation of doping during the growth of the substrates. On the other hand, the fabrication of multilayer porous structures with a controlled spatial design was achieved by anodization of MOCVD grown GaN, with two different electrical conductivities of layers. By anodization of ZnO crystals, the selectivity of ZnO micro-nano-structures obtaining with different shapes was demonstrated. Pyramidal microstructures were obtained on the O face, and inverted pyramids were produced on the Zn face. It was shown that the dimensions of microstructures can be controlled by varying the applied potential during anodization, thus demonstrating a strong influence on the photoluminescence spectra of the obtained microstructures.

The successful combination of electrochemical etching and pulsed electrodeposition led to the solution of an important technological problem, namely, the possibility of non-lithographic fabrication of two-dimensional periodic metal-dielectric structures for micro-opto-electronic and photonic applications, an important precondition for this achievement being the development of the so-called "hopping electrodeposition" mechanism of Au nanodots.

In premiere, the "abnormal" retroreflection of light from ultra-porous layers based on *n*-InP and *n*-GaAs semiconductor compounds was demonstrated. As a result, the following regularities were established: (i) Only ordinary transverse waves ("bright modes") and their associated backscattered radiation can be excited with an incident

s-polarized wave. Absorption strongly modifies the scattering indicatrix, suppressing scattered radiation at small incidence/scattering angles. (ii) Ultrashort modes ("dark modes") and ordinary transverse waves ("bright modes"), as well as their associated backscattered radiation, can be excited with an incident *p*-polarized wave. The contribution from "dark modes", which is practically independent of absorption, is predominant at high incidence/scattering angles.

Using the developed "hopping electrodeposition" model, a cost-effective and original approach for assessing the electrical conductivity in InP semiconductor nanostructures with different thicknesses, such as those fabricated by electrochemical etching of *n*-InP crystals with free carrier concentration of 1.3×10^{18} cm^{-3}, was proposed. The given approach has also been shown to be effective for highlighting non-uniform doping during HVPE growth in GaN substrates. Complementarily, non-uniform doping was also demonstrated by electrochemical etching of GaN (HVPE) substrates. The developed "hopping electrodeposition" model was used for Au nanodot functionalization of promising ZnO or aero-GaN micro- and nano-structures as platforms for the fabrication of 3D hybrid micro-nano-architectures.

It has been shown that combining possibilities to produce two types of pores (CLO and CO) with generating porous arrays by design significantly enlarges the variety of produced porous morphologies and topologies. As a result, possibilities to control the physical properties of semiconductor porous structures, such as optical, vibrational, photonic and luminescence properties, are widened, therefore opening new prospects for practical applications. The systematized results demonstrated that rectangular, triangular, and circular shape of pores, as well as nanowires with controlled sizes can be produced by adjusting the crystallographic orientation of the substrate and the technological conditions of anodization. The optimization of technological parameters of anodization allowed the fabrication of semiconductor nanowire arrays by electrochemical etching of InP, GaAs and ZnTe semiconductor crystals. The use of GaAs crystals with different crystallographic orientation allowed to obtain nanowire arrays tilted (100), perpendicular (111)B and predominantly parallel (001) to the substrate surface by electrochemical etching at applied voltage 4 V in nitric acid with a concentration of 1M for 30 min.

An important compartment of semiconductor compound engineering has been demonstrated which consists in the development of electrochemical technological approaches to control the direction of pore propagation both in depth, being produced 3D structures as a result of the transition from CLO to CO pores, or due to non-uniform doping in GaN HVPE grown substrates, as well as parallel to the surface of InP or ZnSe crystals by applying photolithographic masks. Using the properties of CLO pores to not intersect during growth, combined with the formation of pore networks propagating in planes parallel to substrate surface, were

obtained morphologies by-design determined by the shape of photolithographic mask used, which open new perspectives for microfluidic applications. An additional tool for such applications is the possibility to control the hydrophilic or hydrophobic properties of the produced structures. It has been demonstrated by contact angle analysis that the engineering of semiconductor surfaces by electrochemical methods (etching and/or electrochemical deposition) allows the controlled change of hydrophilic/hydrophobic properties. It was demonstrated that the morphology of GaAs pores, tilted or perpendicular to the surface, plays an important role in the transition from hydrophobic to hydrophilic properties, demonstrating contact angles of 137.5° and 37.5° respectively. Even greater flexibility of contact angle control was demonstrated by functionalization of porous layer with a monolayer of Au nanodots.

Some applications of the elaborated semiconductor nanostructures fabricated by electrochemical methods have been demonstrated, such as the varicap device based on GaP-metal nanocomposites, photodetectors and gas sensors based on InP nanowall and GaAs single nanowire, the exploration of magnetic properties of GaAs-Fe and GaAs-NiFe hybrid core-shell nanowire networks fabricated electrochemically, and the use of gold-functionalized micro- and nanostructures as platforms for creating 3D hybrid micro-nano architectures based on semiconductors.

Based on the systematized findings, the following **recommendations** are proposed:

It remains to be understood why no CO pores are generated in II-VI semiconductor compounds and solid solutions, possessing the same sphalerite crystal structure as III-V semiconductor compounds. In fact, this problem was analyzed only from the consideration of the percentage value of the degree of ionicity in the chemical bonds. The reason why CLO pores do not grow in GaAs crystals should also be elucidated.

Despite the fact that photolithographic mask-assisted electrochemical etching is a cost-effective and versatile tool for the preparation of porous structures with specific morphologies, its exploration is still in the primary phase. The obtained results demonstrated that the design of the porous morphology depends on several factors, namely: from how many and which edge of the photolithographic mask is anodized; size and location of open holes in photolithographic mask, etc. It is proposed to develop a mathematical model for simulation with visualization of anodization results through photolithographic mask with a special design, which, reaching a desired morphology as a result of the simulation, can be repeated experimentally. The following laws and parameters can be recommended as boundary conditions for the simulation: (i) pores can be formed in the space under the specially designed photolithographic mask; (ii) in CLO pore formation regime,

which assumes that the pores cannot intersect each other; (iii) once the thickness of 60 nm is reached, the pores change their propagation direction in the free (non-etched) semiconductor space but in the same plane (these concrete values depend on the conductivity of the material). In the case of the meeting of two neighboring pores tip-to-tip, they will stop growing, leaving a space of 60 nm between them. (iv) the growth rate for all pores is constant, regardless of the number of edges of the photolithographic mask.

Since electrochemical etching is carried out by breaking the chemical bonds between atoms due to the extraction of electrons, it is recommended to carry out the anodization process by combining it with surface charge lithography, which involves the additional introduction of negative charges on the surface that stop the material dissolution process, being previously demonstrated on MOCVD grown GaN substrates [66]. Thus, supplying the surface with excess free charges in a controlled manner will allow to expand the possibility of engineering porous semiconductor compounds.

Acknowledgment

The work is carried out as part of the postdoctoral project for period 2021-2022 „Micro- and nano-engineering of semiconductor compounds based on electrochemical technologies for electronic and photonic applications" with the code #21.00208.5007.15/PD and was partially supported by the institutional subprogram 02.04.02 no. 4/FI «Development of technologies and investigation of the properties of layered semiconductor compounds, hybrid nanostructures and laser sources».

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