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Parallel encoding-decoding of matroid error-correcting codes

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Abstract

The algorithm of parallel encoding and decoding of the maximum distance separable matroid codes is proposed. The parity-check matrices with specific structures are applied for synthesis majority-logic circuits of locating and correcting errors. The parameterized VHDL-entities for implementation of the encoder and decoder are designed.

Keywords: matroid codes, parity-check matrices, encoders, decoders

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