# Multidimensional Digital Signal Processing for Printed Circuit Boards Testing

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**Abstract — A new method for multidimensional digital signal processing for Printed Circuit Boards (PCB) testing is described. The considered method comes to solve such problems as competition and synchronization, which are present in the multidimensional signals processing. The solution is achieved by performing in parallel all operations, replacing the analog-to-digital conversion (ADC) with differentiation operations and analyzing the signal variation rate based on the Fuzzy logic elements. As a result of these operations, using digital integration models, binary code streams are obtained that allow the reconstruction of the signal shape. Mathematical models applied for the transformation and processing of multidimensional signals are presented. The designed system for the multidimensional signal processing consists of a computing unit, the test signals generator, the data storage unit, the Printed Circuit Board with nodes for test signals application and retrieval, and finally the processing elements for differentiation and analysis based on Fuzzy logic.**

***Keywords — multidimensional signal, digital signal processing, PCBs testing, Fuzzy logic, FPGA, ADC.***

## I. INTRODUCTION

Multidimensional signals are present in all aspects of our lives. Because of the immense relevance of signal processing and the fast-growing requirements of industry and business, the most important topics in this domain are signal processing analysis and architectures design. Currently, a lot of mathematical methods and models are developed for multidimensional signal processing with applications in various fields, such as medicine (2D and 3D image processing), industry (Multi-Input Multi-Output systems), economics and management (Data Mining, OLAP), etc.

From a mathematical point of view, any process can be defined in a multidimensional space with an absolute or relative coordinate system through a lot of variables depending on the coordinate system [1, 2, and 3].

An important area for the application of multidimensional signal processing methods and models can be considered the Printed Circuit Boards (PCB) functional and parametric testing. In this case, the PCB can be considered as a Multi-Input Multi-Output system that evaluates in a 2D space, if the board has a one-layer conductive pattern, and 3D, if the board is multi-layer [4, 5, and 6].

The PCBs testing requires a complex multilateral approach that ensures the identification of hardware defects at the topology and logical levels and those at the level of dynamic and transient processes. All these operations can be performed sequentially, with limited resources and at a low cost, or in parallel, using a complex and very expensive systems.

Dynamic and transient processes that occur in PCBs are concurrent processes that require the generation of multiple test signals at the same time with the acquisition of another set of state signals that determine the result of signals-propagation in PCB conductors.

Therefore, the notion of concurrency for PCBs testing is a decisive factor that will determine the correctness of this operation. Respectively, having a Printed Circuit Board with $N$ test nodes also requires $N$ analog-to-digital converters with very high frequency to ensure the detection of delays and transient processes.

In [7, 8] the method of system synthesis for parallel multidimensional signals acquisition and processing for performing the Printed Circuit Boards testing is described. The system contains a lot of homogeneous input channels that perform in parallel data acquisition.

Methods of modeling and synthesis of PCBs testing systems based on Hardware Petri nets implemented into FPGA circuits are described in [9, 10]. The application of Hardware Petri nets models for PCBs testing ensures the validation of the testing system before it is implemented in reconfigurable circuits.

In this paper, a method for digital processing of multidimensional signals for Printed Circuit Boards testing is proposed. The method ensures the simultaneous generation of input signals on the board, the acquisition and concurrent processing of test signals, excluding the analog-to-digital conversion.

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## II. Problem Statement

Let's consider a Printed Circuit Board (Figure 1) with: a set of nodes $U^{In} = \{u_i^{In}, \forall i = \overline{1,N}\}$, $(N = 7)$, that represents the input signal vector; a set of nodes $U^{Out} = \{u_j^{Out}, \forall j = \overline{1,K}\}$, $(K = 8)$ that denotes the vector of functional and parametric test signals, where the analytical model for $U^{Out}$ signal calculation is defined as $u_j^{Out} = g_j(U^{In}, Z_j)$; the matrix of electrical impedances generated by the respective conductors $Z = [Z_{i,j}, \forall i = \overline{1,N}, j = \overline{1,K}]$, where $Z_{i,j} = f_{i,j}(R_{i,j}, L_{i,j}, C_{i,j}), \forall i = \overline{1,N}, j = \overline{1,K}$, $f_{i,j}$ is the calculation formula in which $R_{i,j}$ represents the electrical resistance of the conductor, $L_{i,j}$ is the conductor inductance and $C_{i,j}$ is the electrical capacity of the conductor.

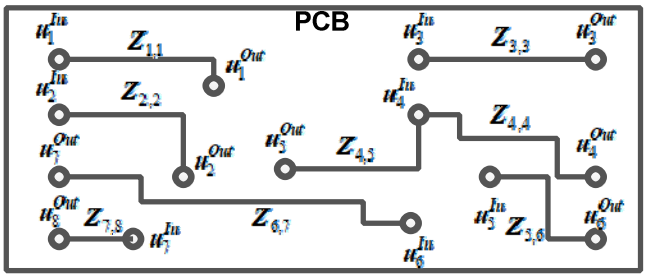


Fig. 1. Printed Circuit Board.

In our research, we propose to develop a system that allows PCBs testing using input signal $U^{In}$ generation models, concurrent acquisition of multidimensional output signals $U^{Out}$ and their digital processing to identify the influence of the electrical signal propagation process in the conductors and their mutual influence.

## III. Functional Block Diagram of the System

Figure 2 shows the functional block diagram of the system for Printed Circuit Board testing based on the digital processing of multidimensional signals.

The functional block diagram consists of: a computing unit ***PC*** that contains the environment for the development and programming FPGA circuits and the tool for multidimensional signals digital processing; ***FPGA TSG*** - FPGA circuit configured according to test signal generator (vector $U^{In}$); ***PCB*** - Printed Circuit Board to be tested, with inputs $U^{In}$ and outputs $U^{Out}$; $du_j^{Out}/dt$ - elements of time differentiation, calculate the speed of signals variation at the PCB outputs (vector $U^{Out}$); $A\dot{U}^{Out}$ - amplification elements and Fuzzy logic units that encode the speed of output signal variation and generate a binary code $Y$; ***FPGA SAP*** - FPGA circuit configured according to data stack and interface for data transfer to ***PC***; ***SYN*** - synchronization block of the data storage process.

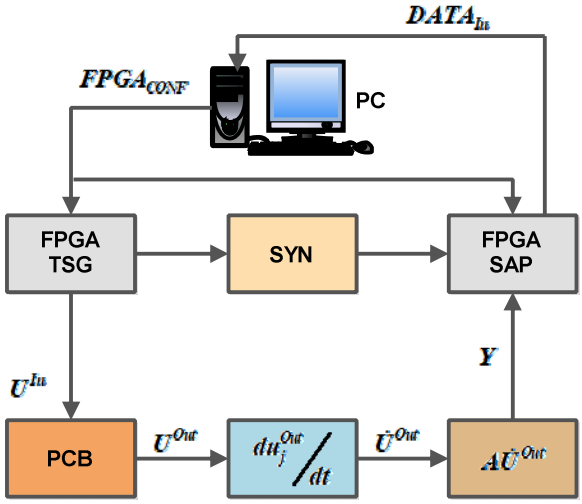


Fig. 2. Functional block diagram.

## IV. Fuzzy Logic Unit Block Diagram

The functional block diagram of the Fuzzy logic unit is presented in Figure 3.

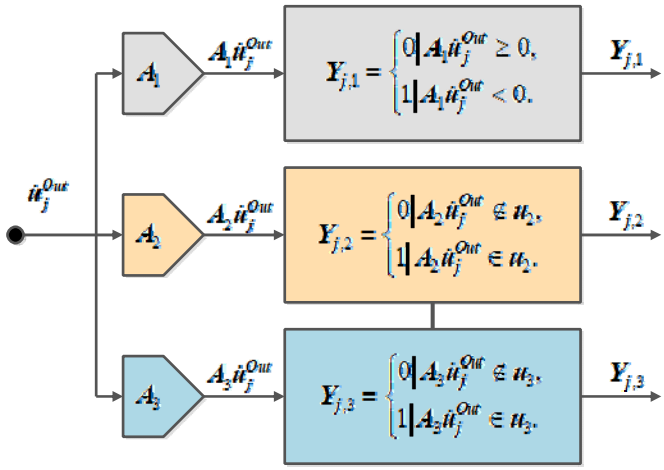


Fig. 3. Fuzzy logic unit block diagram.

The Fuzzy logic unit transforms the variation speed and polarity of the output signal $\dot{u}_j^{Out}$ into binary code. The set of amplifiers $A_1, \ldots A_3$ boosts the $\dot{u}_j^{Out}$ signal level to the analysis level $A_l \dot{u}_j^{Out}, \forall l = \overline{1,3}$. The bit $Y_{j,1}$ determines the sign of the binary code (positive – 0 and negative - 1). The bits $Y_{j,2}$ and $Y_{j,3}$ represents the binary code of the output signal speed variation.

Depending on the working frequency of the Printed Circuit Board, the sampling step for the Fuzzy logic is calculated. Table I presents the approximation codes.