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Room temperature bonding for vacuum applications: climatic and long time tests

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Abstract A detailed and quantitative motivation for the necessity of room temperature (RT) bonding for wafer level packaging of silicon micro-mirrors will be given. Results on RT 6 inch wafer bonding with vacuum encapsulation on test structures are presented. Structured as well as unstructured wafers have been bonded at RT using a Mitsubishi Heavy Industries bonder. Unstructured wafers were used for the determination of the bonding strength, whereas the structured wafers were used for the evaluation of vacuum level and its stability with time.

1 Introduction

Many different types of micro-electromechanical systems (MEMS) chips require wafer level packaging (WLP). The main driving forces for WLP are the protection of the chips against the hazardous environment during dicing and the cost efficiency of the WLP process (Baert et al. 2004). Many WLP processes are based on wafer bonding (Tong and Goessele 1998) and are normally done in the back end of line, i.e. at a time when the chips are completely processed and are composed of many materials with different thermal coefficients of expansion. The so called state of the art bonding methods like glass frit, anodic, eutectic etc. require a tempering process usually above 300 °C. This tempering process during the bonding procedure is a challenge for the fully integrated chips. Each tempering process will induce an additional mechanical stress, which can lead to yield or reliability disadvantages (Choa 2005).

The most often in the literature mentioned argument why WLP should be done at temperatures below 400 °C, are the Al interconnections which start to show reliability problems if treated at temperatures above 400 °C. However, there are additional reasons why low temperature bonding methods are required for MEMS WLP. Due to their micromechanical parts, MEMS chips are more sensitive as compared with pure electrical chips. For example, in the case of silicon micro-mirrors a temperature treatment after the release of the mirrors can lead to the change in the planarity and roughness of the metal-coated silicon mirrors, which can consequently affect the final optical properties, e.g. reflectivity, of the device (Hsu et al. 2008).

2 Tempering effects on micro-mirrors

In Fig. 1 an example is presented where 30 μm thick and 1.5 mm in diameter crystalline Si micro-mirrors were tempered at temperatures starting from 150 up to 450 °C. Seven groups have been used for the experiments (groups B to H). Every group, eight chips each, was tempered for 1 h at a certain temperature. Corresponding temperature profiles for each group are presented in Fig. 1a. Before and after the tempering process the radius of curvature and the roughness of micro-mirrors was measured by means of a White Light Interferometer (WLI). The WLI results are presented in Fig. 1b.

As can be observed, the radius of curvature before the tempering process has a relatively high spread and a mean value of slightly above 10 m. The tempering process significantly decreases the radius of curvature. Already at 150 °C the radius of curvature decreases by more than 4 m,

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